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# ILS\_RISA

## ENE micom

CPU : INTEL CEDARVIEW-M

Chip Set : INTEL TIGERPOINT

Remarks : DC, DDR3

Model Name : ILS\_RISA  
 PCB Part No : BA41-01968A(GCE)  
                   BA41-01969A(HANNSTAR)  
                   BA41-01970A(PIOTEK)

Dev. Step : MP

Revision : 1.1

T.R. Date : 2011.12.20

DRAW	CHECK	APPROVAL
Qin Wenchao	Wu shijiang	BL LEE

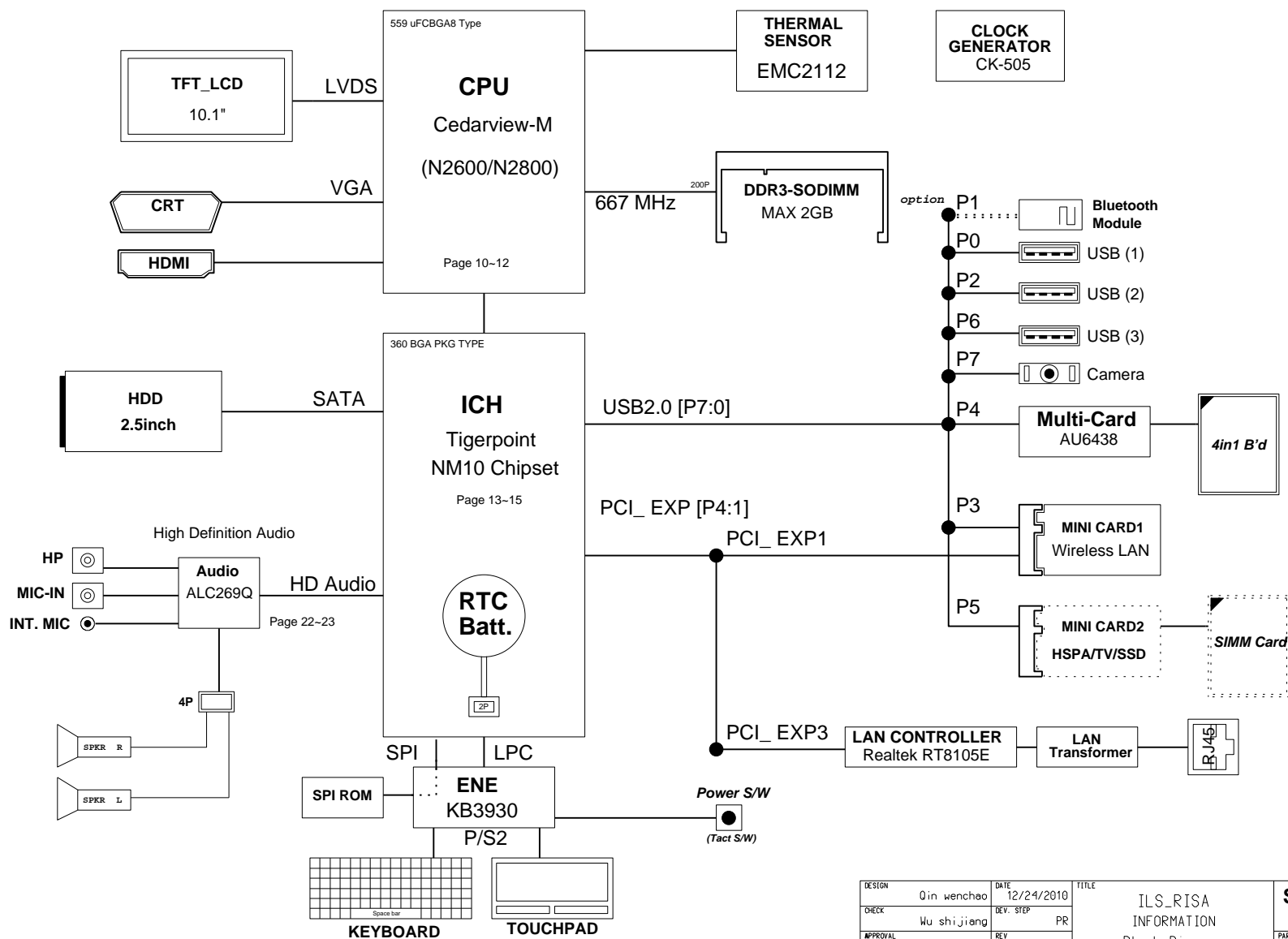
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DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	SAMSUNG
CHECK	Wu shijiang	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	BL LEE	REV	1.0		COVER	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	1	OF 44

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**OPERATION BLOCK DIAGRAM**

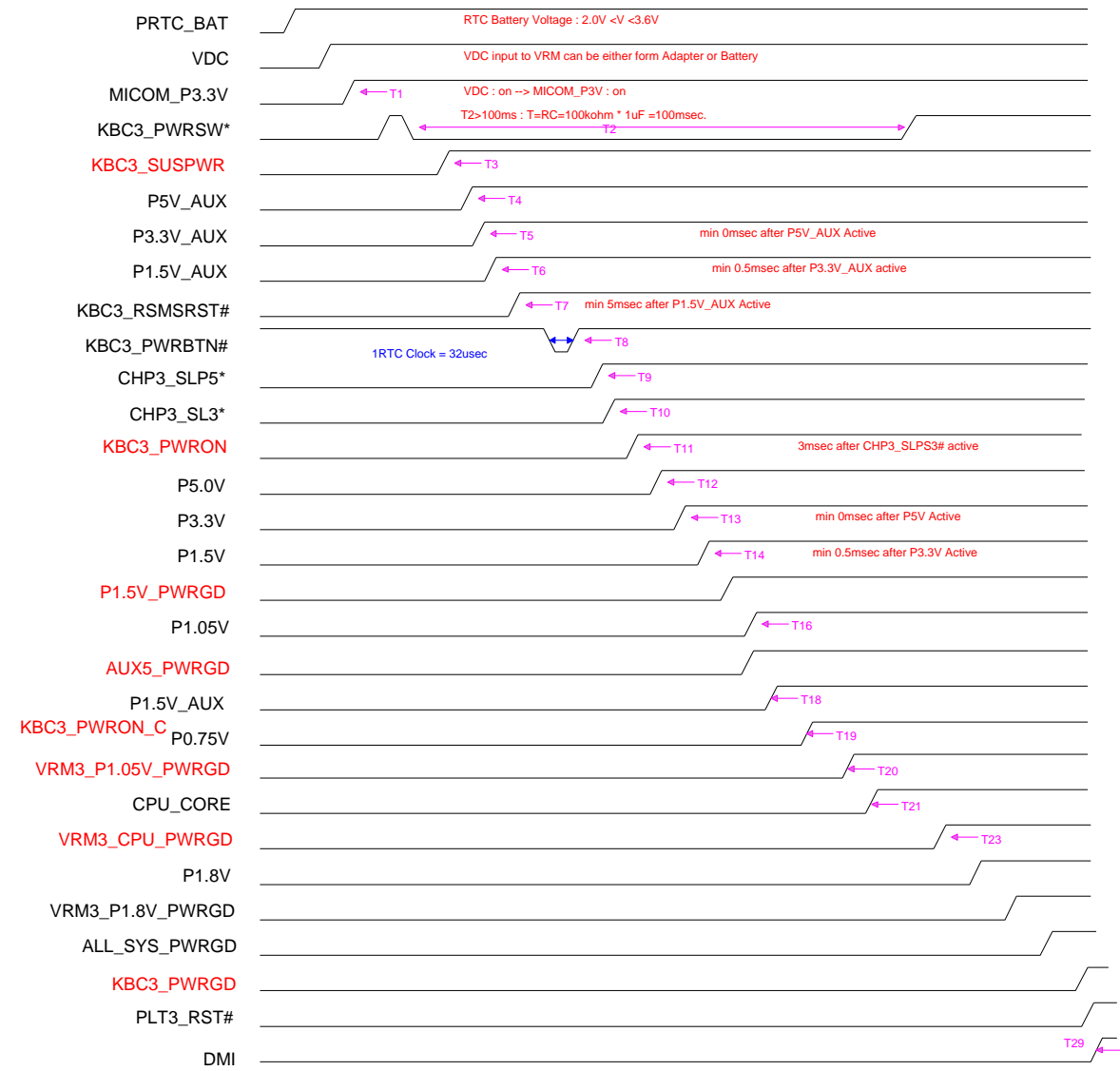
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CHECK	Wu shijiang	DEV. STEP	PR			PART NO. BA41-0XXXXA
APPROVAL	BL LEE	REV	1.0			
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# BOARD INFORMATION

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### Power Sequence Timing



### PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB Hub to PCI OK-505M (Clock Generator) SODIMM0 CPU Thermal Sensor	AD29(internal) AD30(internal) AD31(internal) AD24(internal)	Programmable	

### I<sup>2</sup>C / SMB Address

Devices	Address	Hex	Bus
TigerPoint	Master		SMBUS Master
OK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	
CPU Thermal Sensor	0111 101X	7Ah	Thermal Sensor

### USB PORT Assign

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0 0	USB Port(Debug port)	UHCL_2 4	CardBus Cont.
UHCL_0 1	Touchscreen Pannel	UHCL_2 5	Bluetooth Module
UHCL_1 2	USB Port	UHCL_3 6	USB Port(Chargeable)
UHCL_1 3	Mini Card (For WLAN/WWAN)	UHCL_3 7	CAMERA

### PCI Express Assign

Port Number	ASSIGNED TO
1	Mini Card 1(Wireless LAN)
2	Mini Card 2 (HSDPA/Wibro)
3	LOM

### Voltage Rails

Power Rail	Descriptions
PRTC_BAT	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well.
VDC	Primary DC system power supply (9 to 19V)
P1.05V(VCCP)	VTT for CPU, Callistoga & ICH7-M
P3.3V_MICOM	3.3V always power rail(for Micom)
P1.5V_AUX	1.5V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
CPU_CORE	Core voltage for Atom CPU

DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA INFORMATION Board Information	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			PART NO. BA41-0XXXXA
APPROVAL	BL LEE	REV	1.0			
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**POWER DIAGRAM**

Rev 1.0

**KBC3\_SUSPWR**  
**(KBC3\_PWRSW#)**
**KBC3\_PWRON**  
**(CHP3\_SLPS3\*)**
**VRM3\_P1.05V\_PWRGD**

AC Adapter

Battery DC

**VDC****P3.3V\_MICOM**

MICOM

**P5.0V\_ALW****P12.0V\_ALW****P1.5V\_AUX**SODIMM (DDR III)  
CALISTOGA**P0.75V**

DDR III-Termination

**P5.0V\_AUX****P3.3V\_AUX**PCH LAN  
TPM P1.8V\_VRM**P1.05V\_LAN**

LAN

**P1.05V**N2100/N2600  
NM10 Chipset**CPU\_CORE**

N2100/N2600

**P5.0V**Thermal LVDS  
SATA Touchpad  
CPU\_VRM**P1.5V**CLK generator  
Cedarview  
Tigerpoint**P3.3V**CLK generator  
DDR LVDS  
Audio PCMCIA  
SSD TPM  
CPAS\_LED FFS**P1.8V**

Cedarview

Power On/Off Table by S-state

Rail State	S0	S3	S4	S5
+V*A(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	—	—
+1.5V_AUX +0.75V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

**S5-S4****S3****S0**

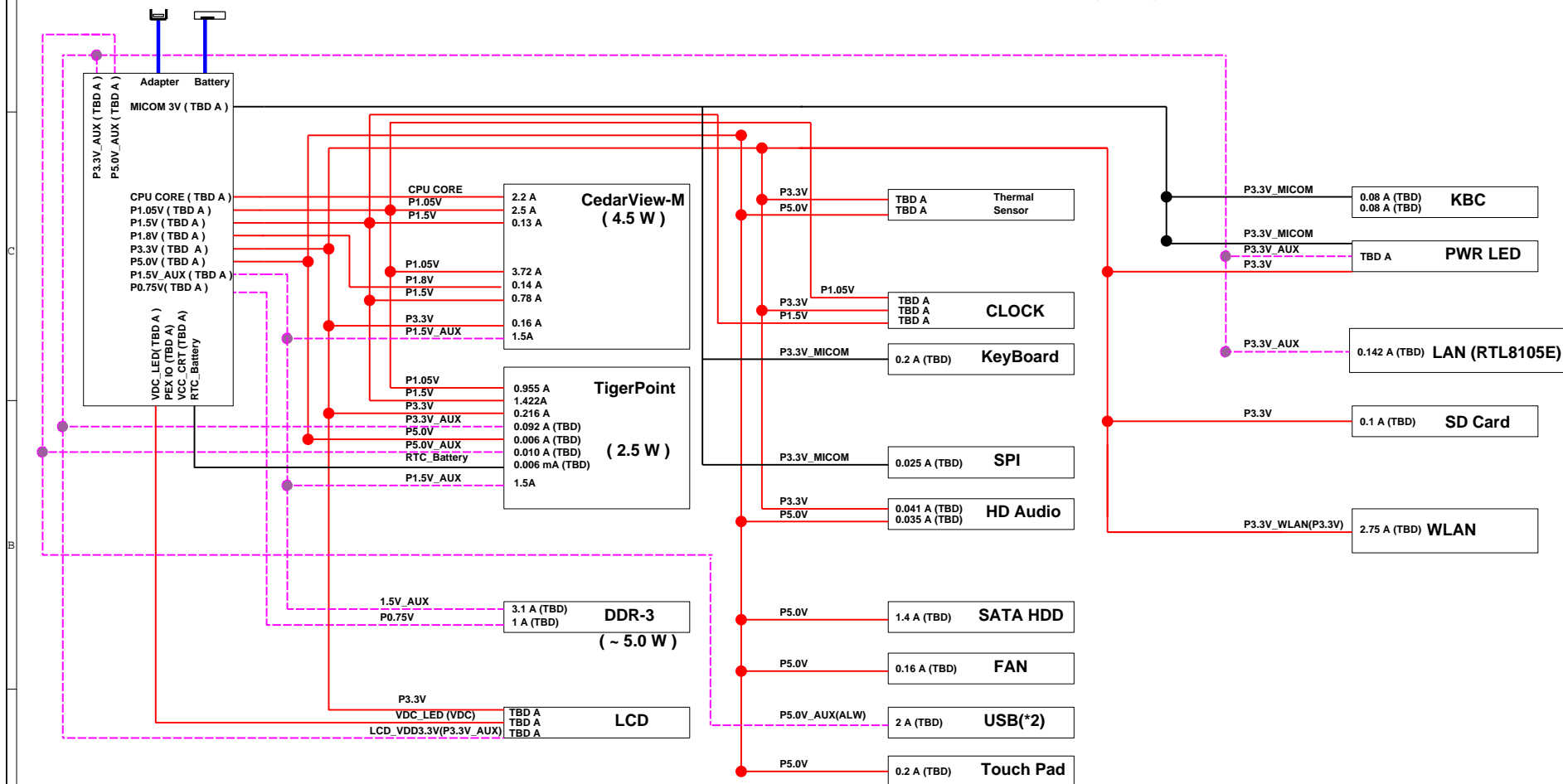
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APPROVAL	BL LEE	LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	4	OF 44

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**POWER RAILS ANALYSIS**

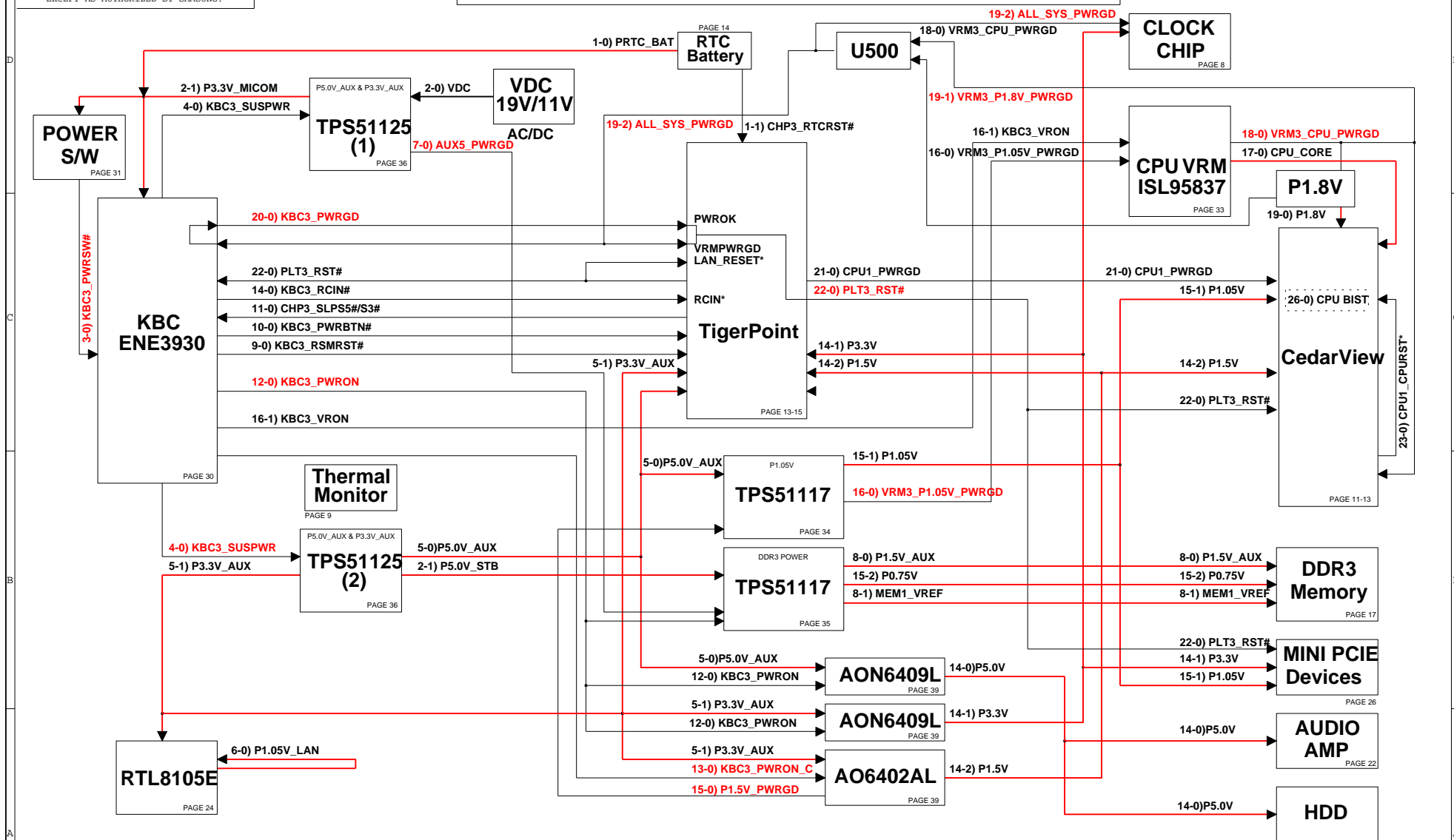
Rev. 1.0 (060920)



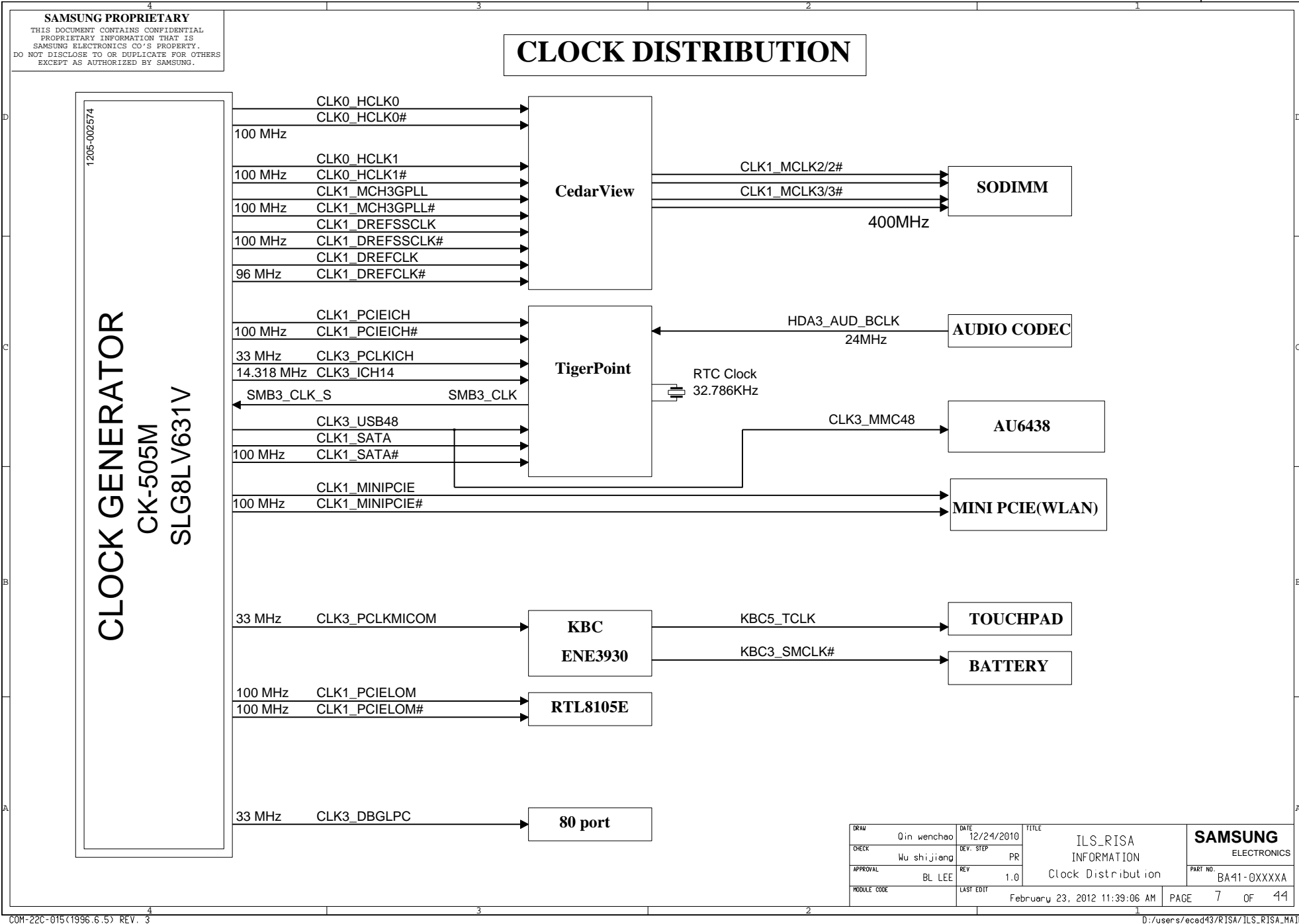
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MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	5 OF 44	

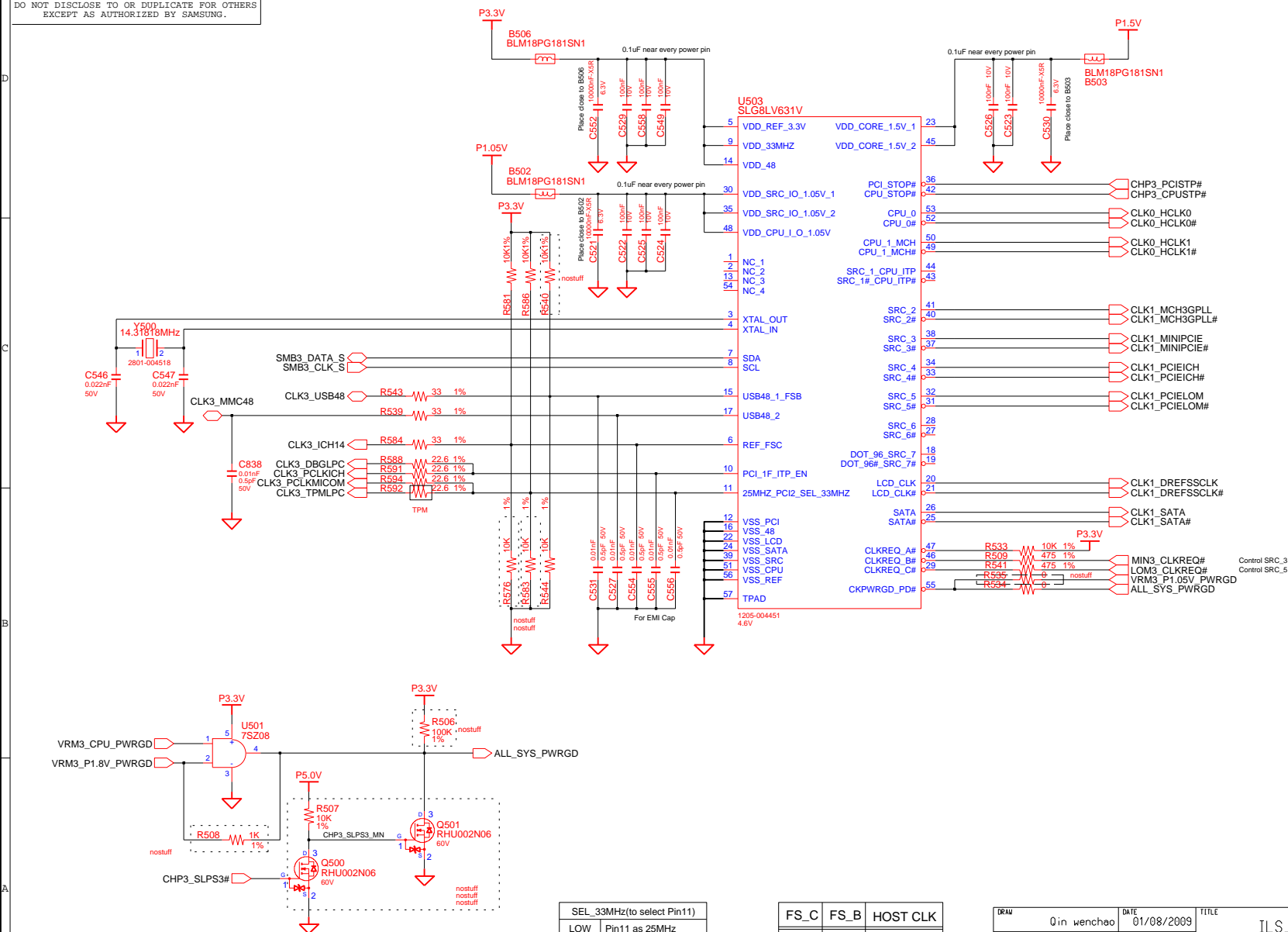
# POWER SEQUENCE BLOCK DIAGRAM

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DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	INFORMATION		
APPROVAL	BL LEE	REV	1.0	Power Sequence Block	PART NO.	
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SEL_33MHz(to select Pin11)	
LOW	Pin11 as 25MHz
HIGH	Pin11 as 33MHz

FS_C	FS_B	HOST CLK
0	0	133 MHz
0	1	166 MHz
1	1	200 MHz
1	0	100 MHz

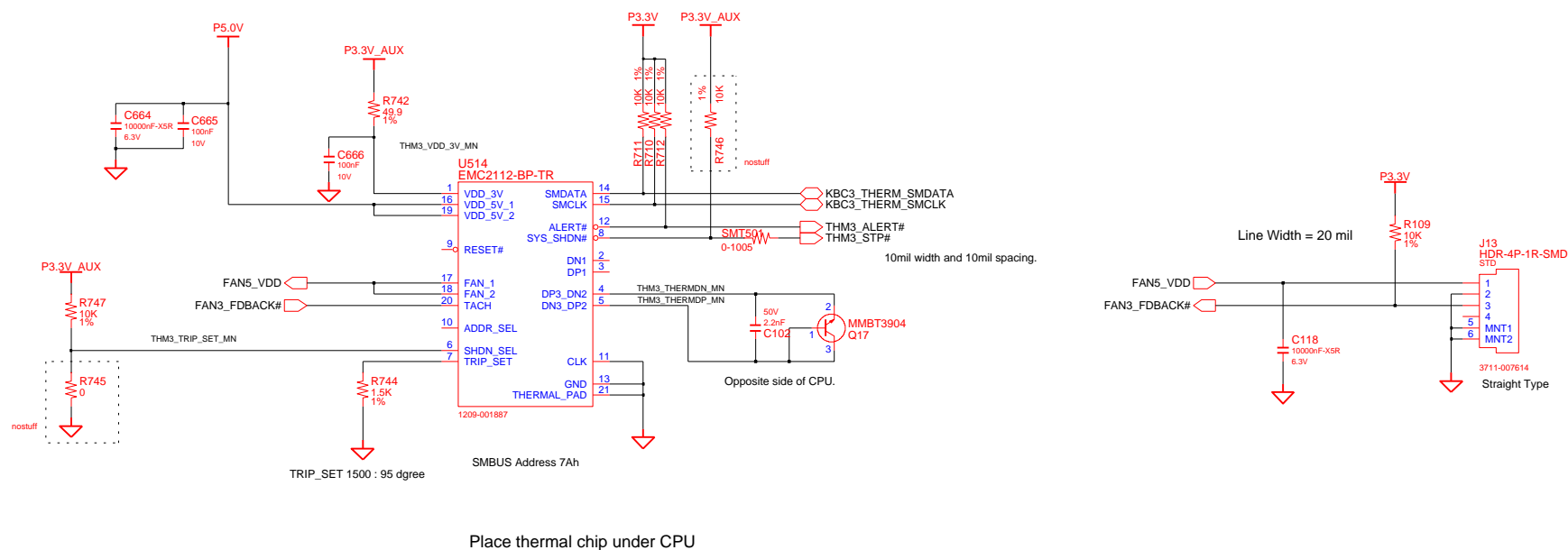
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APPROVAL	BL LEE	REV	1.0					
MODULE CODE	undefined	LAST EDIT		February 23, 2012 11:39:06 AM	PAGE	8 OF 44		



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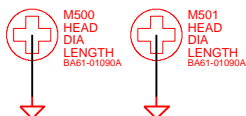
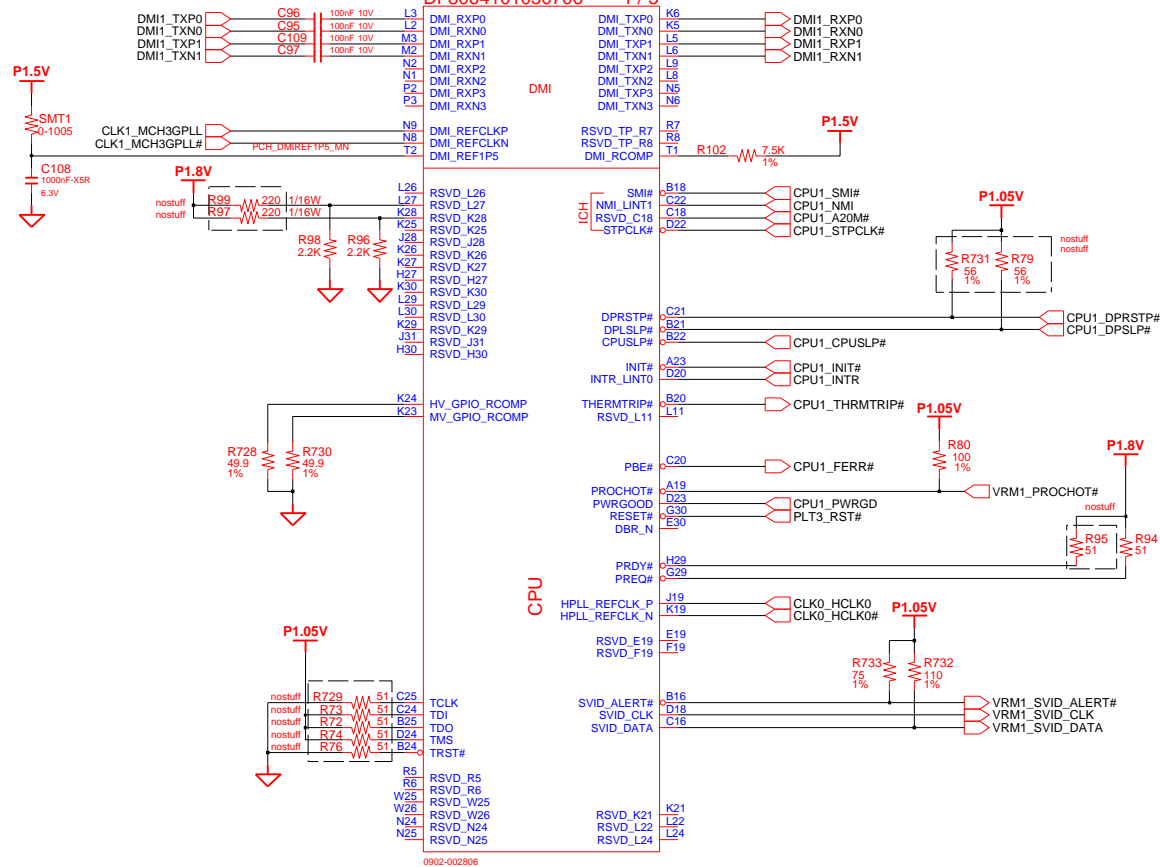
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# THERMAL SENSOR & FAN CONTROL



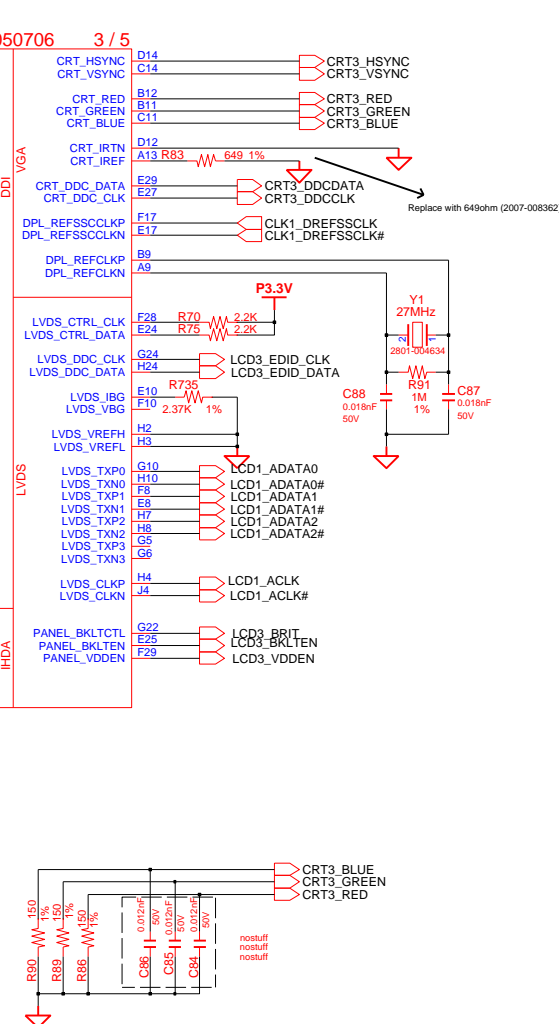
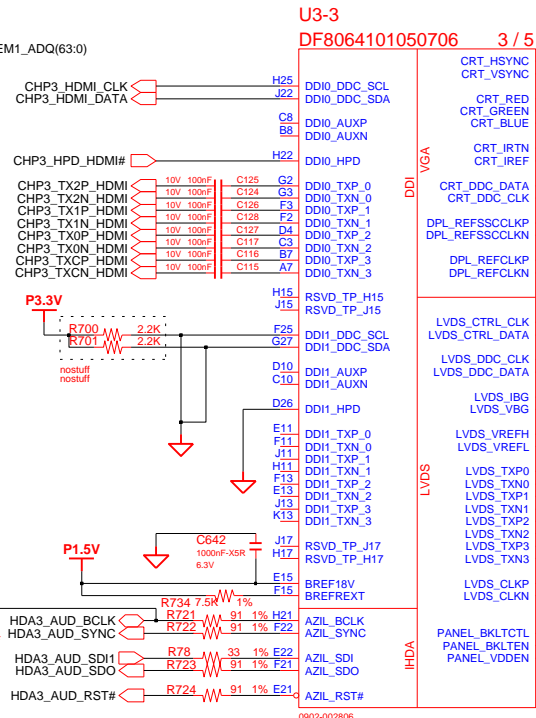
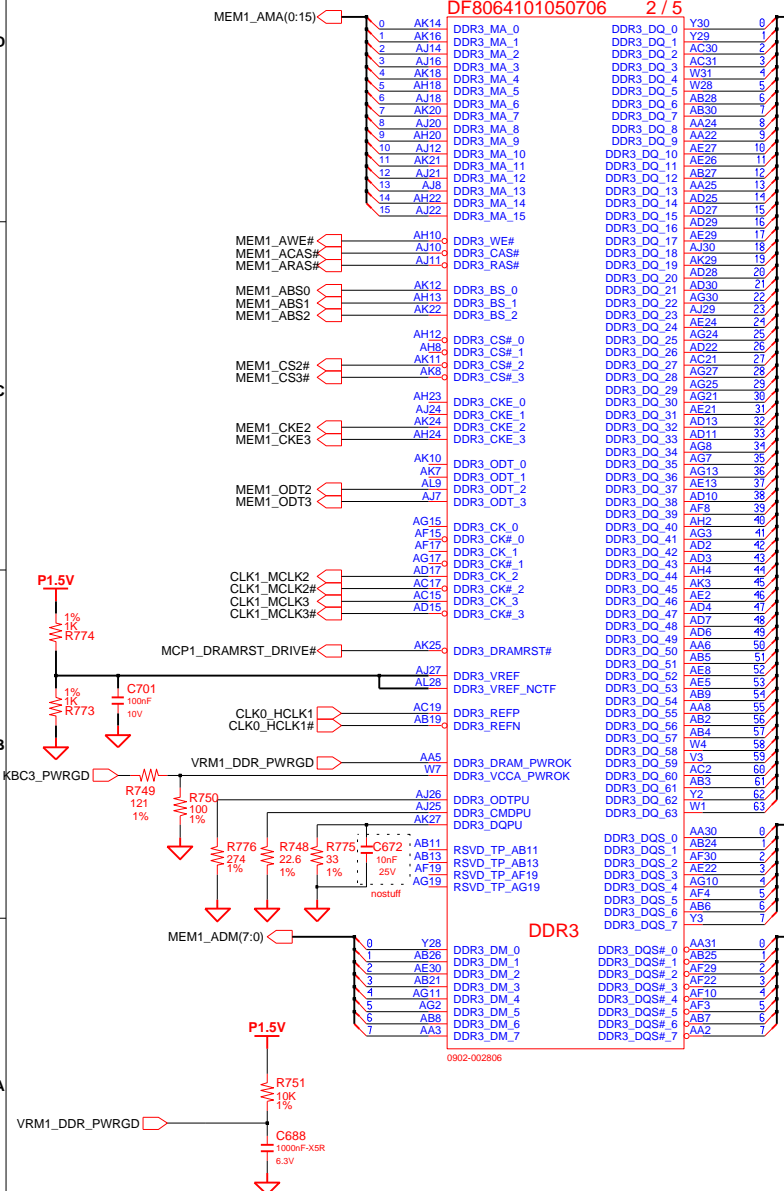
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APPROVAL	BL LEE	REV	1.0		THERMAL SENSOR EMC2112	
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM		PAGE 9 OF 44	

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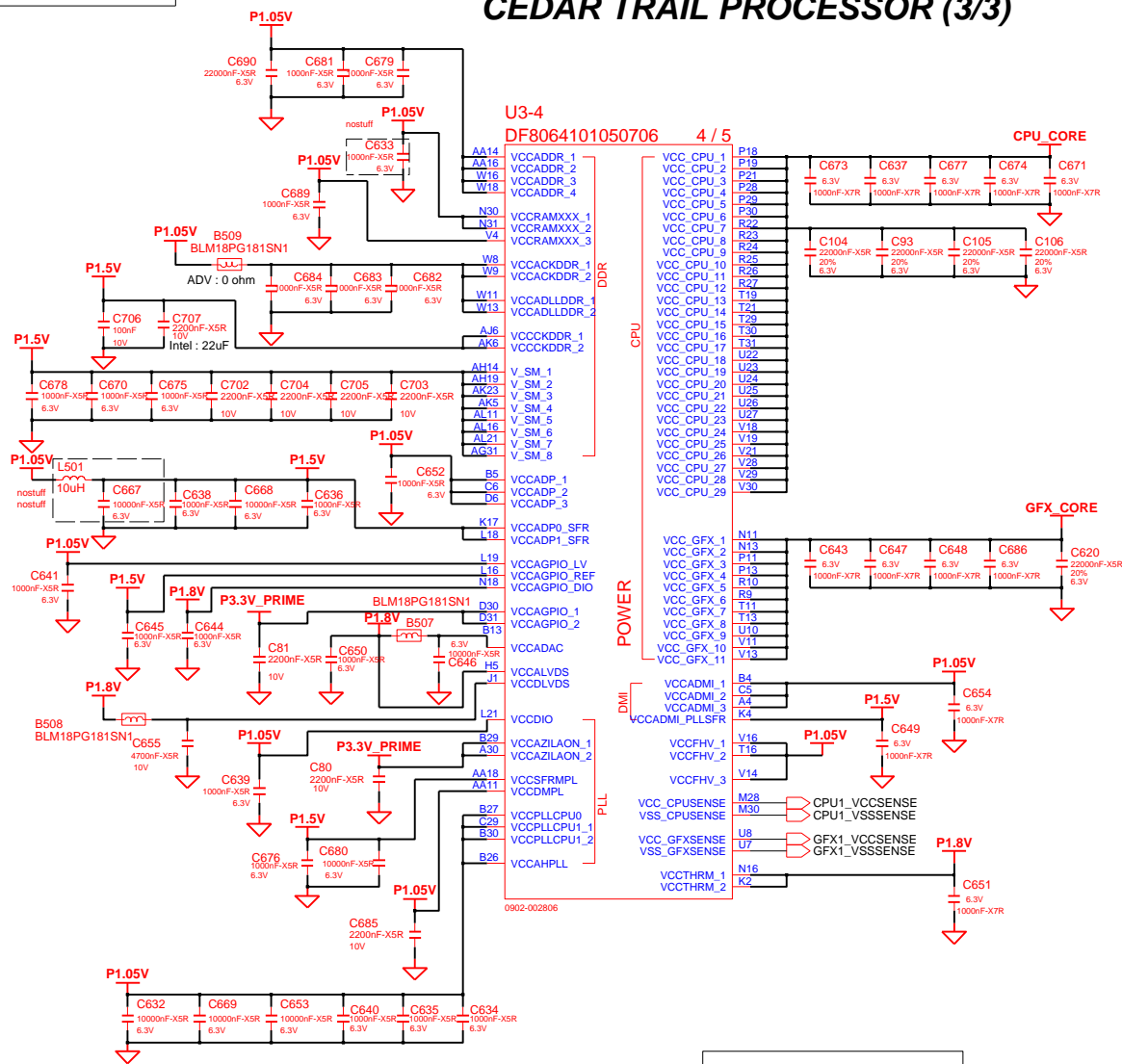
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CHECK	Wu shijiang	DEV. STEP	PR		
APPROVAL	BL LEE	REV	1.0		
MODULE CODE			LAST EDIT		
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DESIGN	Qin wenchao	DATE	11/16/2010	TITLE  ILS_RISA  CPU  Cedar View(2/3)	SAMSUNG  ELECTRONICS
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APPROVAL	BL LEE	REV	1.0		
MODULE CODE	LAST EDIT				
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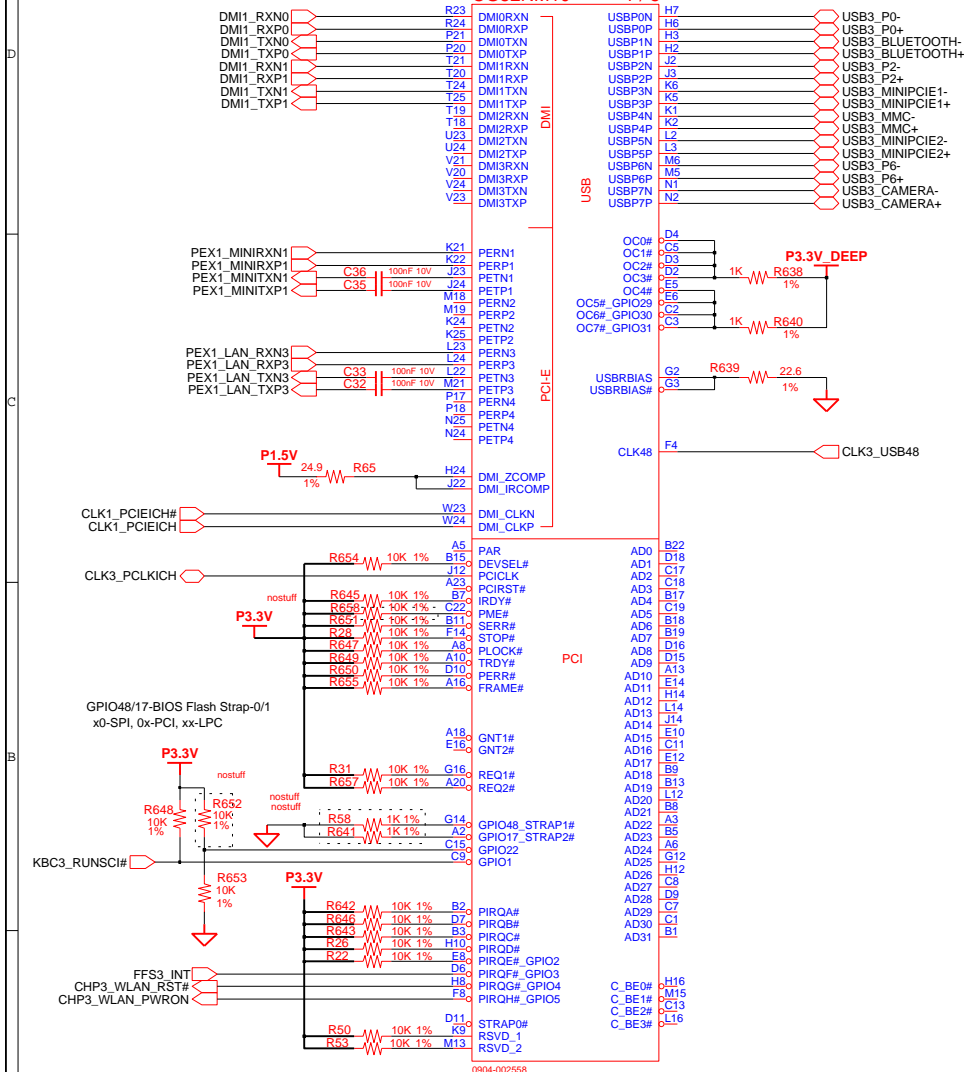
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DF8064101050706 / 5



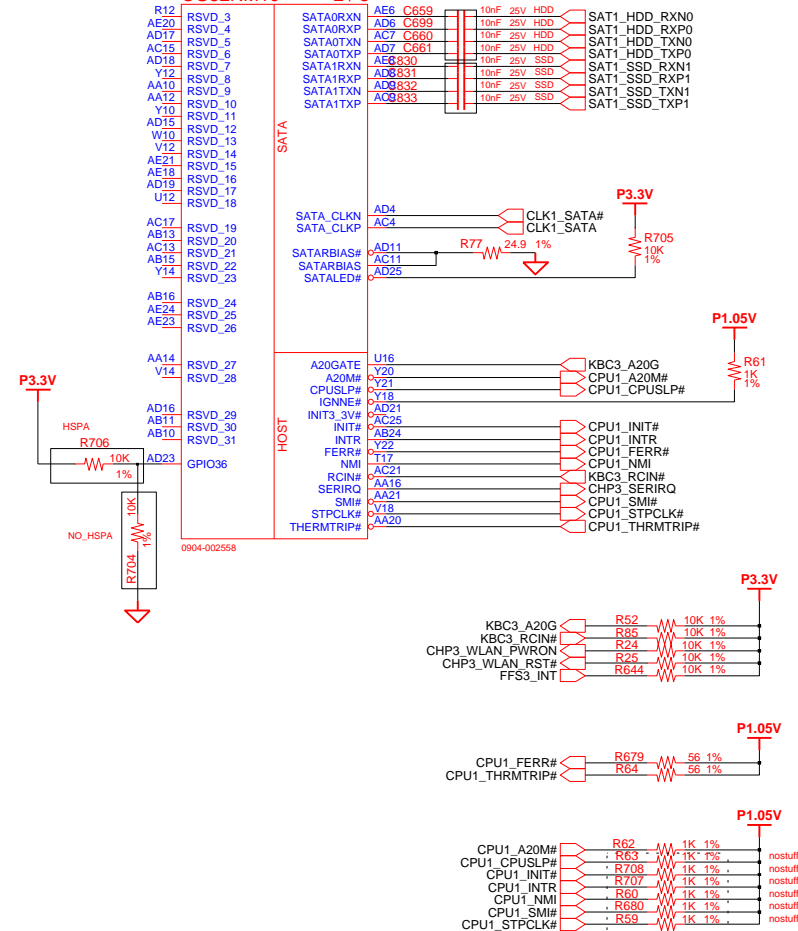
A11	VSS. 1	VSS. 91	H19
A16	VSS. 2	VSS. 92	H20
A21	VSS. 3	VSS. 93	H28
A25	VSS. 4	VSS. 94	H6
A11	VSS. 5	VSS. 95	J2
A10	VSS. 6	VSS. 96	J21
A13	VSS. 7	VSS. 97	J10
AA19	VSS. 8	VSS. 98	J30
AA21	VSS. 9	VSS. 99	K11
AA3	VSS. 10	VSS. 100	K15
AA26	VSS. 11	VSS. 101	K7
AA27	VSS. 12	VSS. 102	K3
AA7	VSS. 13	VSS. 103	K8
AA9	VSS. 14	VSS. 104	L1
AB15	VSS. 15	VSS. 105	L1
AB17	VSS. 16	VSS. 106	L13
AB17	VSS. 17	VSS. 107	L23
AB23	VSS. 18	VSS. 108	L25
AB29	VSS. 19	VSS. 109	L31
AC1	VSS. 20	VSS. 110	M7
AC10	VSS. 21	VSS. 111	L7
AC11	VSS. 22	VSS. 112	M29
AC13	VSS. 23	VSS. 113	M4
AC22	VSS. 24	VSS. 114	N10
AC28	VSS. 25	VSS. 115	N11
AD1	VSS. 26	VSS. 116	N19
AD4	VSS. 27	VSS. 118	N21
AD21	VSS. 28	VSS. 118	N22
AD24	VSS. 29	VSS. 119	N26
AD5	VSS. 30	VSS. 120	N23
AD6	VSS. 31	VSS. 121	N27
AD5	VSS. 32	VSS. 122	N28
AE1	VSS. 33	VSS. 123	N4
AE10	VSS. 34	VSS. 124	N7
AE11	VSS. 35	VSS. 125	P14
AE15	VSS. 36	VSS. 126	P16
AE17	VSS. 37	VSS. 127	P4
AE19	VSS. 38	VSS. 128	T18
AE3	VSS. 39	VSS. 129	T3
AE31	VSS. 40	VSS. 130	T11
AF11	VSS. 41	VSS. 131	U5
AF13	VSS. 42	VSS. 132	U9
AF21	VSS. 43	VSS. 133	W2
AF24	VSS. 44	VSS. 134	W10
AF4	VSS. 45	VSS. 135	W12
AF7	VSS. 46	VSS. 136	W14
AG22	VSS. 47	VSS. 137	W19
AG5	VSS. 48	VSS. 138	W21
AH26	VSS. 49	VSS. 139	W22
AH28	VSS. 50	VSS. 140	W21
AH6	VSS. 51	VSS. 141	W23
AH9	VSS. 52	VSS. 142	W24
AJ3	VSS. 53	VSS. 143	W30
AK13	VSS. 54	VSS. 144	W27
AK19	VSS. 55	VSS. 145	W6
AK28	VSS. 56	VSS. 146	W4
AK9	VSS. 57	VSS. 147	
AL13	VSS. 58		
AL19	VSS. 59		
AL23	VSS. 60	VSS. 148	A27
AL27	VSS. 61	VSS. 149	A29
AL26	VSS. 62	VSS. 150	AH1
B10	VSS. 63	VSS. 151	AJ1
B14	VSS. 64	VSS. 152	AJ1
B14	VSS. 65	VSS. 153	AJ1
B19	VSS. 66	VSS. 154	AJ1
B21	VSS. 67	VSS. 155	AK2
B24	VSS. 68	VSS. 156	AK30
C26	VSS. 69	VSS. 157	AK1
C30	VSS. 70	VSS. 158	AL28
C7	VSS. 71	VSS. 159	AL3
D19	VSS. 72	VSS. 160	AL30
D28	VSS. 73	VSS. 161	AL5
D6	VSS. 74	VSS. 162	B2
D9	VSS. 75	VSS. 163	B3
E2	VSS. 76	VSS. 164	B31
E5	VSS. 77	VSS. 165	C1
F24	VSS. 78	VSS. 166	C1
F4	VSS. 79	VSS. 167	C2
G1	VSS. 80	VSS. 168	G1
G11	VSS. 81	VSS. 169	
G13	VSS. 82		
G15	VSS. 83		
G15	VSS. 84	VSS. C0VDET	D13
G17	VSS. 85	VSSA.CRTDAC	L14
G19	VSS. 86		
G21	VSS. 87		
G31	VSS. 88		
H8	VSS. 89		
H13	VSS. 90		

DESIGN	Qin wenchao	DATE	11/16/2010	ILS_RISA CPU Cedar View(3/3)	SAMSUNG ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	PR		PART NO.	BA41-0XXXXA
APPROVAL	BL LEE	REV	1.0			
MODULE CODE	LAST EDIT				February 23, 2012 11:39:06 AM	PAGE

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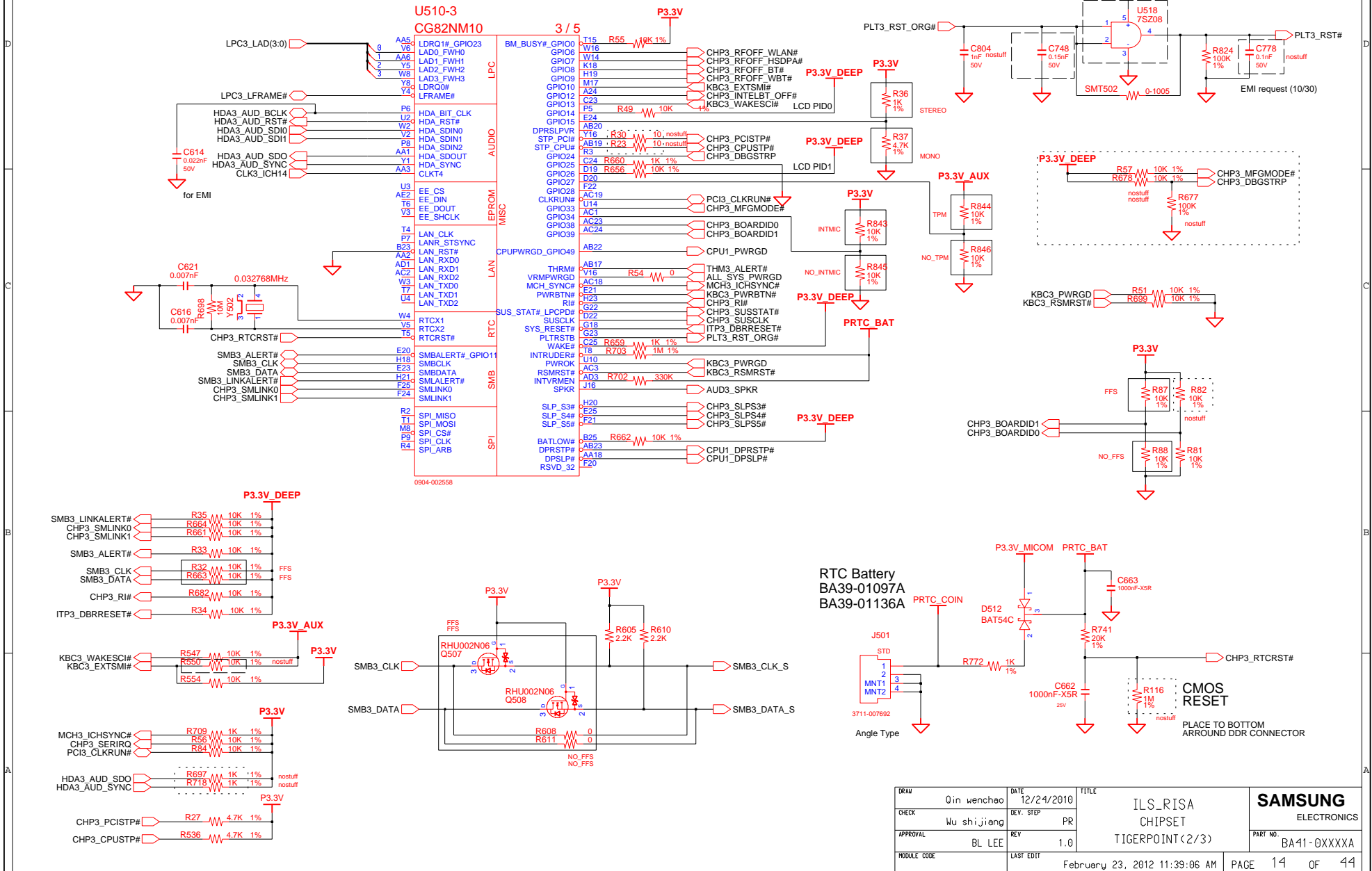
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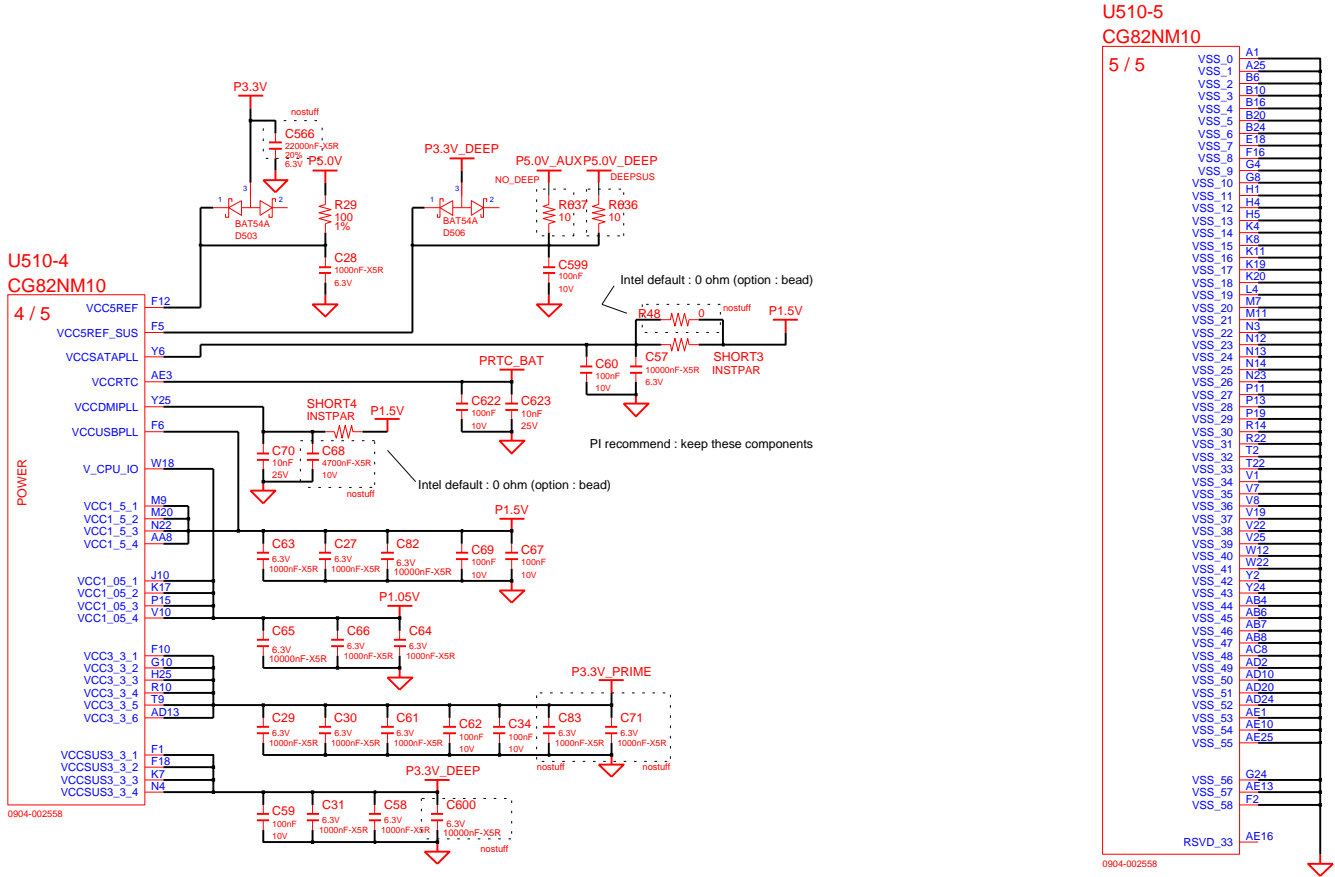
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**Tigerpoint (2/3)**

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Tigerpoint (3/3)



DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA CHIPSET TIGERPOINT(3/3)	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			PART NO. BA41-0XXXXA
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80H DECODER CONNECTOR AND DEBUG CODE  
AMI Aptio 4.x Status Codes

ACPI/ASL Status Codes

- 01 System is entering S1 sleep state
- 02 System is entering S2 sleep state
- 03 System is entering S3 sleep state
- 04 System is entering S4 sleep state
- 05 System is entering S5 sleep state
- 10 System is waking up from the S1 sleep state
- 20 System is waking up from the S1 sleep state
- 30 System is waking up from the S1 sleep state
- 40 System is waking up from the S1 sleep state
- AC System has transitioned into ACPI mode(PIO)
- AA System has transitioned into ACPI mode(ACPI)

PEI Status Codes

Progress Codes

- 10 PEI Core is started
- 11 Pre-memory CPU initialization is started
- 12 Pre-memory CPU initialization(CPU module specific)
- 13 Pre-memory CPU initialization(CPU module specific)
- 14 Pre-memory CPU initialization(CPU module specific)
- 15 Pre-memory North Bridge initialization is started
- 16 Pre-memory North Bridge initialization(North Bridge module specific)
- 17 Pre-memory North Bridge initialization(North Bridge module specific)
- 18 Pre-memory Bridge initialization(North Bridge module specific)
- 19 Pre-memory South Bridge initialization is started
- 1A Pre-memory South Bridge initialization (South Bridge module specific)
- 1B Pre-memory South Bridge initialization (South Bridge module specific)
- 1C Pre-memory South Bridge initialization (South Bridge module specific)
- 1D-2A OEM pre-memory initialization codes
- 2B Memory initialization.Serial Presence Detect (SPD) data reading
- 2C Memory initialization.Memory presence Detection
- 2D Memory initialization. Programming memory timing information
- 2E Memory initialization. Configuring memory
- 2F Memory initialization (other)
- 30 Reserved for ASL (see ASL Status Codes section below)
- 31 Memory Installed
- 32 CPU post-memory initialization is started
- 33 CPU post-memory initialization. Cache initialization
- 34 CPU post-memory initialization. Application Processor(s) (AP) initialization
- 35 CPU post-memory initialization. Boot Strap Processor(BSP) selection
- 36 CPU post-memory initialization. System Management Mode (SMM) initialization
- 37 Post-Memory North Bridge initialization is started
- 38 Post-Memory North Bridge initialization (North Bridge module specific)
- 39 Post-Memory North Bridge initialization (North Bridge module specific)
- 3A Post-Memory North Bridge initialization (North Bridge module specific)
- 3B Post-Memory South Bridge initialization is started
- 3C Post-Memory South Bridge initialization (South Bridge module specific)
- 3D Post-Memory South Bridge initialization (South Bridge module specific)
- 3E Post-Memory South Bridge initialization (South Bridge module specific)
- 3F-4E OEM post memory initialization codes
- 4F DXE IPL is started

PEI Error Codes

- 50 Memory initialization error.Invalid memory type or incompatible memory speed.
- 51 Memory initialization error.SPD reading has failed
- 52 Memory initialization error.Invalid memory size or memory modules do not match
- 53 Memory initialization error.No useable memory detected
- 54 Unspecified memory initialization error
- 55 Memory not installed
- 56 Invalid CPU type or Speed
- 57 CPU mismatch
- 58 CPU self test failed or possible CPU cache error
- 59 CPU micro-code is not found or micro-code update is failed
- 5A Internal CPU error
- 5B Reset PPI is not available
- 5C-5F Reserved for future AMI error codes

S3 Resume Progress Codes

- E8 S3 Resume Failed in PEI
- E9 S3 Resume PPI not Found
- FA S3 Resume Boot Script Error
- EB S3 OS Wake Error
- EC-EF Reserved for future AMI error codes

Recovery Progress Codes

- F0 Recovery condition triggered by firmware(Auto recovery)
- F1 Recovery condition triggered by user(Forced recovery)
- F2 Recovery process started
- F3 Recovery firmware image is found
- F4 Recovery firmware image is loaded
- F5-F7 Reserved for future AMI progress codes

Recovery Error Codes

- F8 Recovery PPI is not available
- F9 Recovery capsule is not found
- FA Invalid recovery capsule
- FB-FF Reserved for future AMI error codes
- 5A Internal CPU error
- 5B reset PPI is not available
- 5C-5F Reserved for future AMI error codes

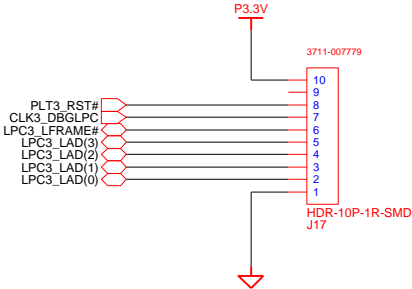
DXE Status Codes

Progress Codes

- 60 DXE Core is started
- 61 NVRAM initialization
- 62 Installation to the South Bridge Runtime Services
- 63 CPU DXE initialization is started
- 64 CPU DXE initialization(CPU module specific)
- 65 CPU DXE initialization(CPU module specific)
- 66 CPU DXE initialization(CPU module specific)
- 67 CPU DXE initialization(CPU module specific)
- 68 PCI host bridge initialization
- 69 North Bridge DXE initialization is started
- 6A North Bridge DXE SMM initialization is started
- 6B North Bridge DXE initialization(North Bridge module specific)
- 6C North Bridge DXE initialization(North Bridge module specific)
- 6D North Bridge DXE initialization(North Bridge module specific)
- 6E North Bridge DXE initialization(North Bridge module specific)
- 6F North Bridge DXE initialization(North Bridge module specific)
- 70 South Bridge DXE initialization is started
- 71 South Bridge DXE SMM initialization is started
- 72 South Bridge devices initialization
- 73 South Bridge DXE initialization(South Bridge module specific)
- 74 South Bridge DXE initialization(South Bridge module specific)
- 75 South Bridge DXE initialization(South Bridge module specific)
- 76 South Bridge DXE initialization(South Bridge module specific)
- 77 South Bridge DXE initialization(South Bridge module specific)
- 78 ACPI module initialization
- 79 CSM initialization
- 7A-7F Reserved for future AMI DEX codes
- 80-8F OEM DEX initialization codes
- 90 Boot Device Selection (BDS) phase is started
- 91 Driver connecting is started
- 92 PCI Bus initialization is started
- 93 PCI Bus Hot Plug Controller Initialization
- 94 PCI Bus Enumeration
- 95 PCI Bus Request Resources
- 96 PCI Bus Assign Resources
- 97 Console Output devices connect
- 98 Console Input devices connect
- 99 Super IO Initialization
- 9A USB initialization is started
- 9B USB Reset
- 9C USB Detect
- 9D USB Enable
- 9E-9F Reserved for future AMI codes
- A0 IDE initialization is started
- A1 IDE Reset
- A2 IDE Detect
- A3 IDE Enable
- A4 SCSI Initialization is started
- A5 SCSI Reset
- A6 SCSI Detect
- A7 SCSI Enable
- A8 Setup Verifying Password
- A9 Start of Setup
- AA Reserved for ASL (see ASL Status Codes section below)
- AB Setup Input Wait
- AC Reserved for ASL (see ASL Status Codes section below)
- AD Ready To Boot event
- AE Legacy Boot Event
- AF Exit Boot Services event
- B0 Runtime Set Virtual Address MAP Begin
- B1 Runtime Set Virtual MAP End
- B2 Legacy Option ROM Initialization
- B3 System Reset
- B4 USB Hot Plug
- B5 PCI Bus Hot Plug
- B6 Clean-up of NVRAM
- B7 Configuration Reset (reset of NVRAM settings)
- B8-BF Reserved for future AMI codes
- C0-CF OEM BDS initialization codes

DXE Error Codes

- D0 CPU initialization error
- D1 North Bridge initialization error
- D2 South Bridge initialization error
- D3 Some of the Architectural Protocols are not available
- D4 PCI resource allocation error.Out of Resources
- D5 No Space for Legacy Option ROM
- D6 No Console Output Devices are found
- D7 No Console Input Devices are found
- D8 Invalid password
- D9 Error loading Boot Option(Loadimage returned error)
- DA Boot Option is failed(Startimage returned error)
- DB Flash update is failed
- DC Reset protocol is not available



DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA SPI BIOS_ROM	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR		80 Debug Port & Code	PART NO. BA41-0XXXXA
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	16	OF 44

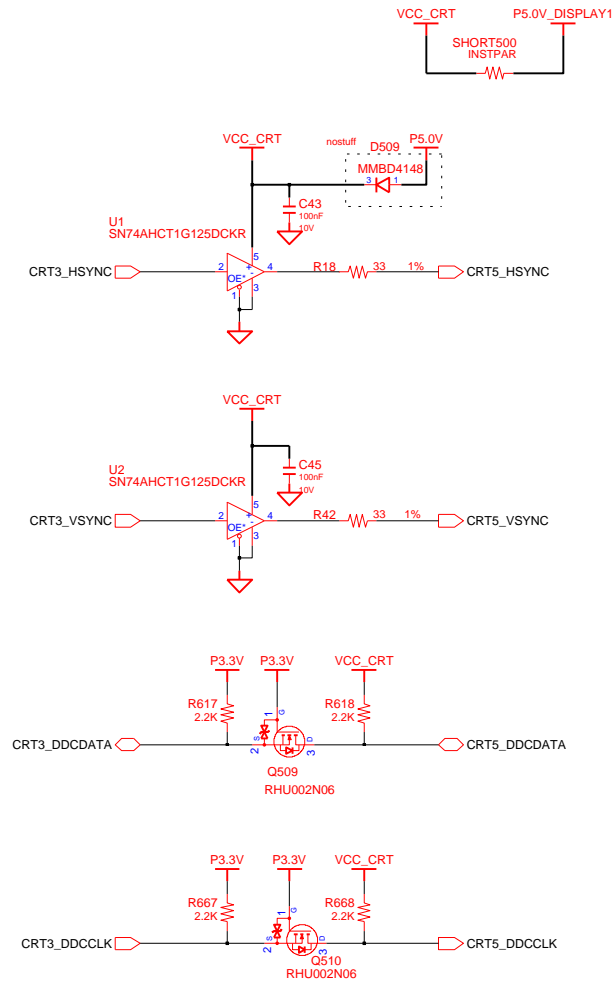




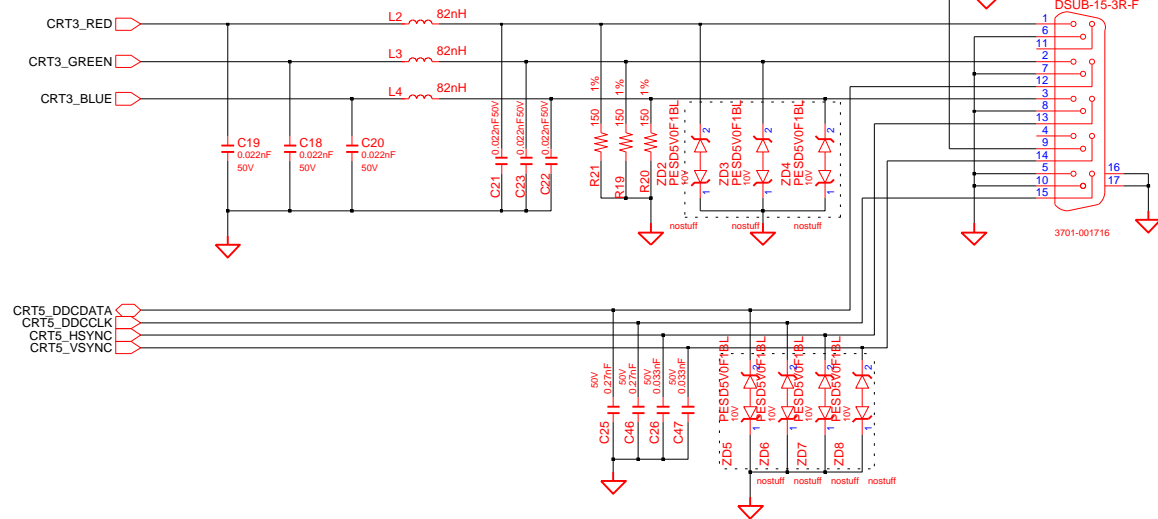
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# CRT



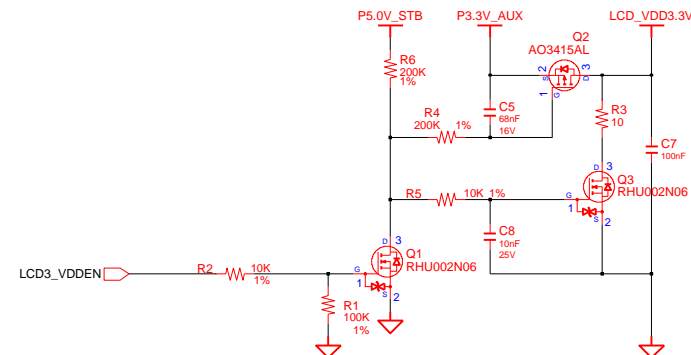
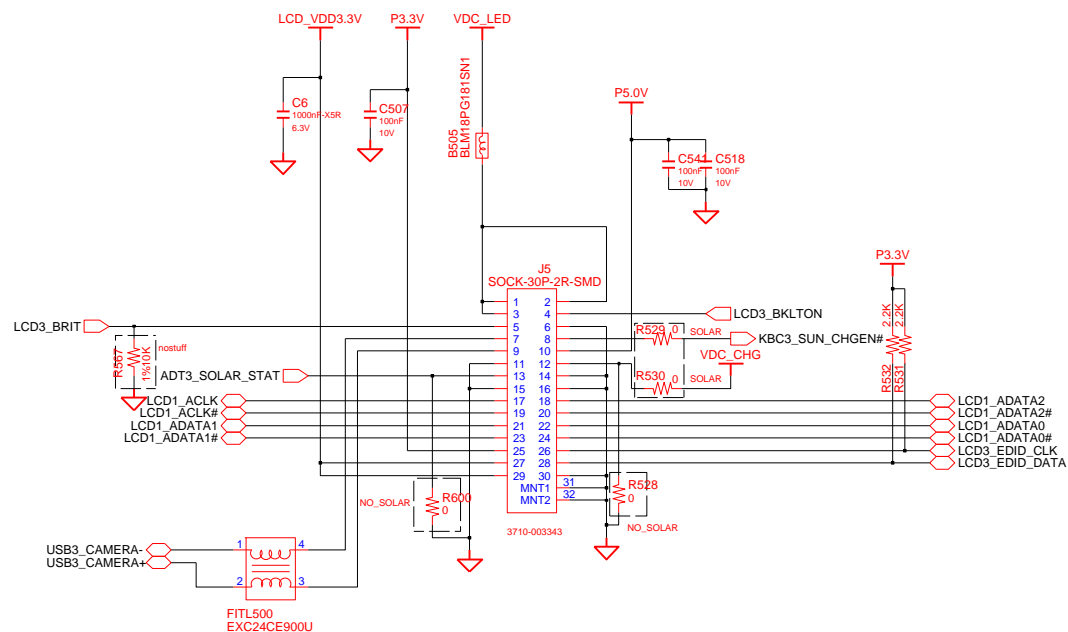
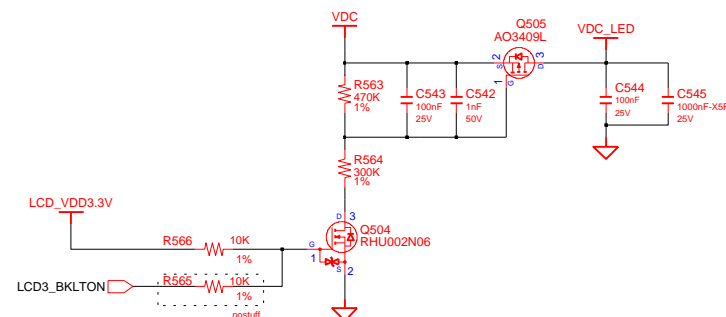
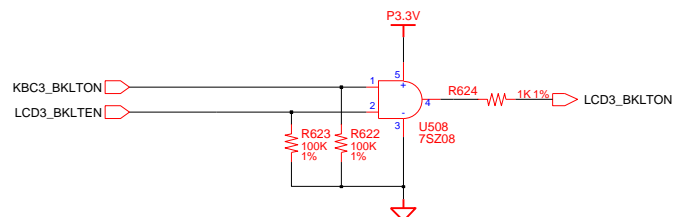
## CRT CONNECTOR



DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA GRAPHICS_IF CRT	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			PART NO. BA41-0XXXXA
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	18	OF 44

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**LCD POWER****LED POWER****Backlight ON**

DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA GRAPHICS_IF LED LCD I/F	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	19 OF 44	

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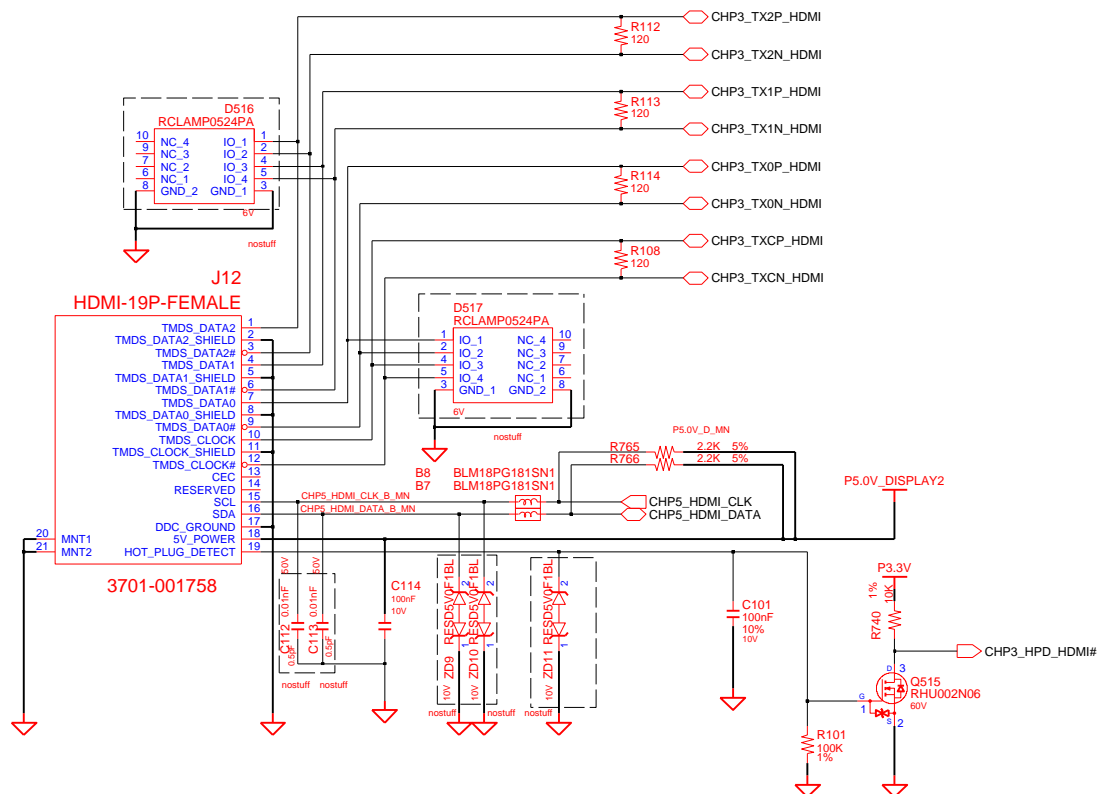
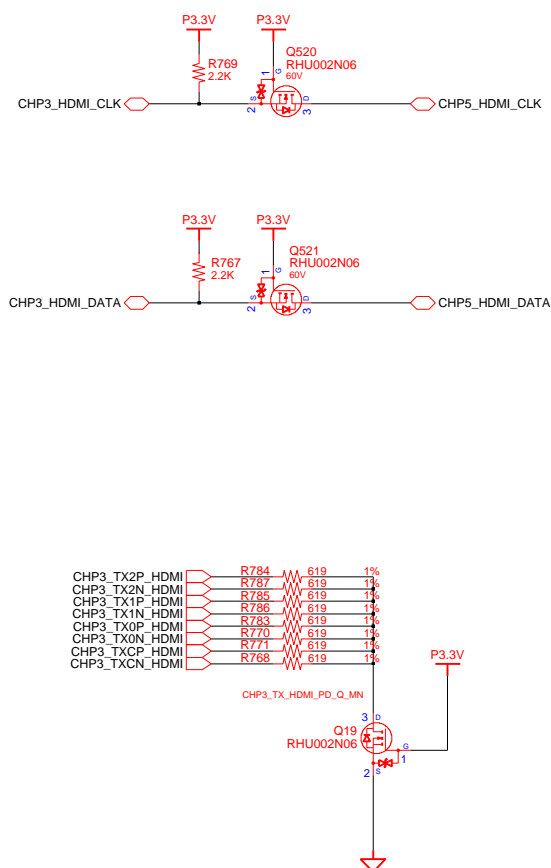
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# HDMI Graphic

After checking, Houston need to use CMC for each signal.

(EMC request at 2010.04.15)

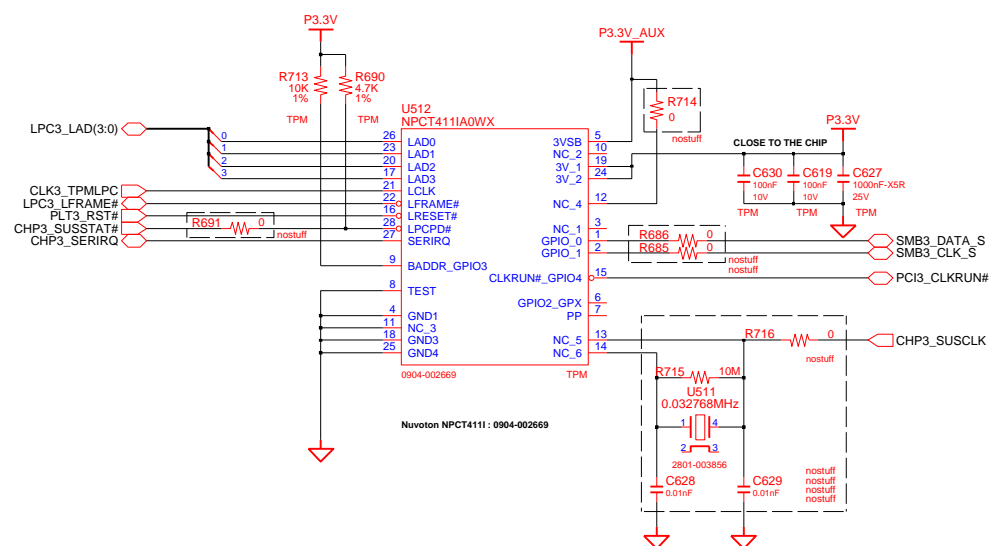
## FOR HDMI VERIFICATION TEST



DESIGN	Qin wenchao	DATE	9/23/2008	TITLE	ILS_RISA	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR		GRAPHICS_IF	
APPROVAL	BL LEE	REV	1.0		HDMI	
MODULE CODE		LAST EDIT				PART NO. BA41-0XXXXA
February 23, 2012 11:39:06 AM						PAGE 20 OF 44

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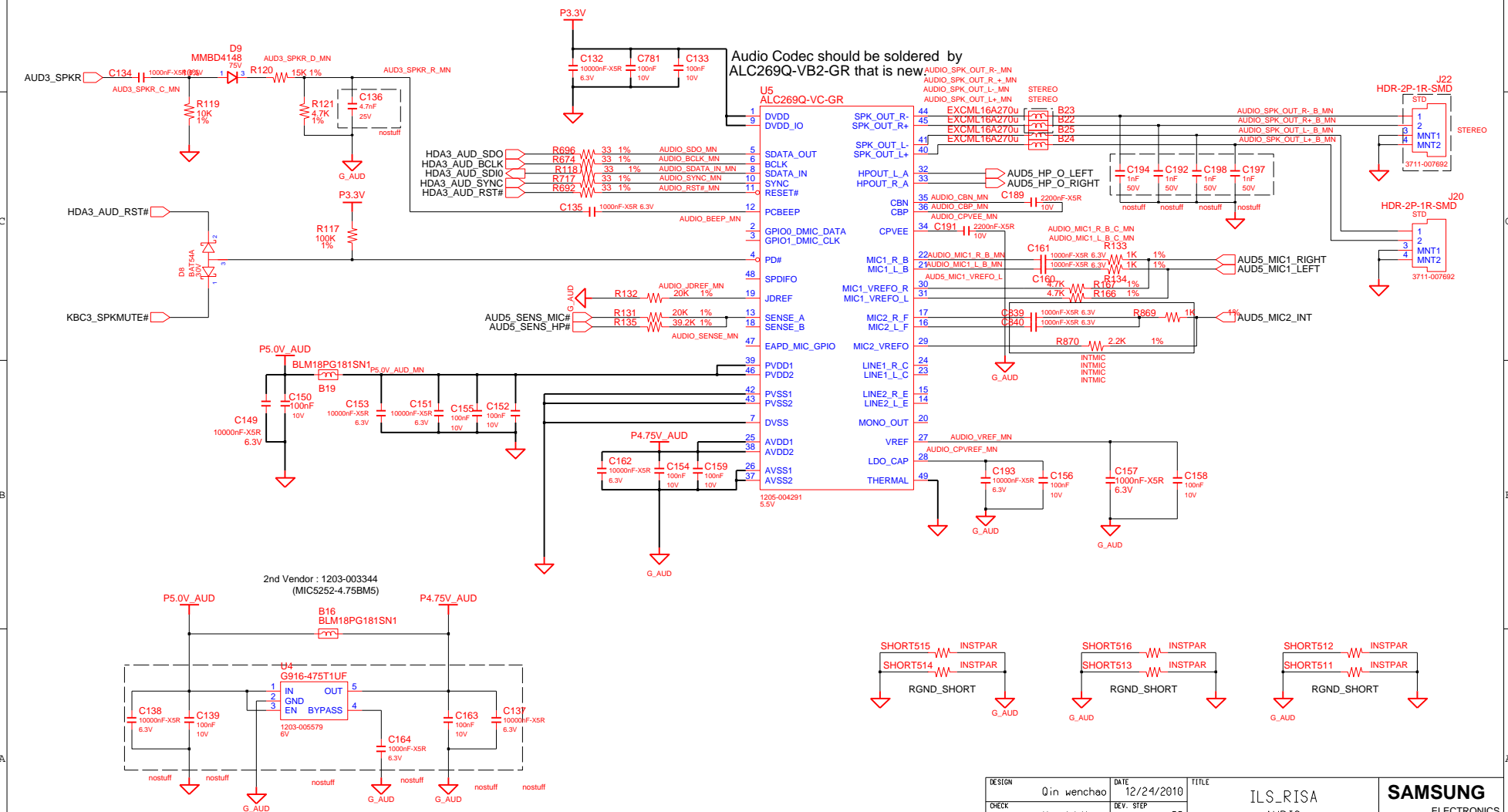
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**TPM 1.2**

DRAW	Qin wenchao	DATE	10/06/2010	TITLE	ILS_RISA	SAMSUNG
CHECK	Wu shijiang	DEV. STEP	PR		TPM	ELECTRONICS
APPROVAL	BL LEE	REV	1.0		TPM1.2	PART NO.
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM			BA41-0XXXXA
				PAGE	21	OF 44

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

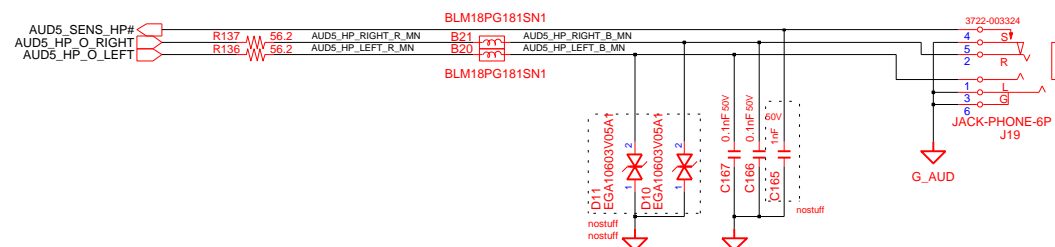
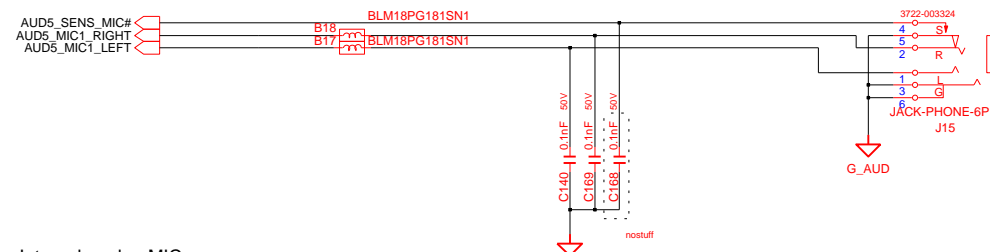
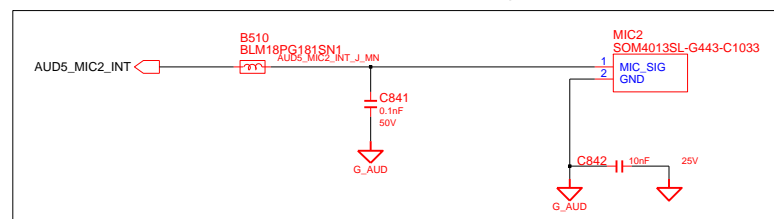
# Audio Codec



DESIGN	Qin wenchao	DATE	12/24/2010	TITLE		<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	REV. STEP	PR			
APPROVAL	BL LEE	REV	1.0	ALC269Q-VC-GR		PART NO. BA14-DXXXXA
MODULE CODE	LAST EDIT		February 23, 2012 11:39:06 AM		PAGE	22 OF 44

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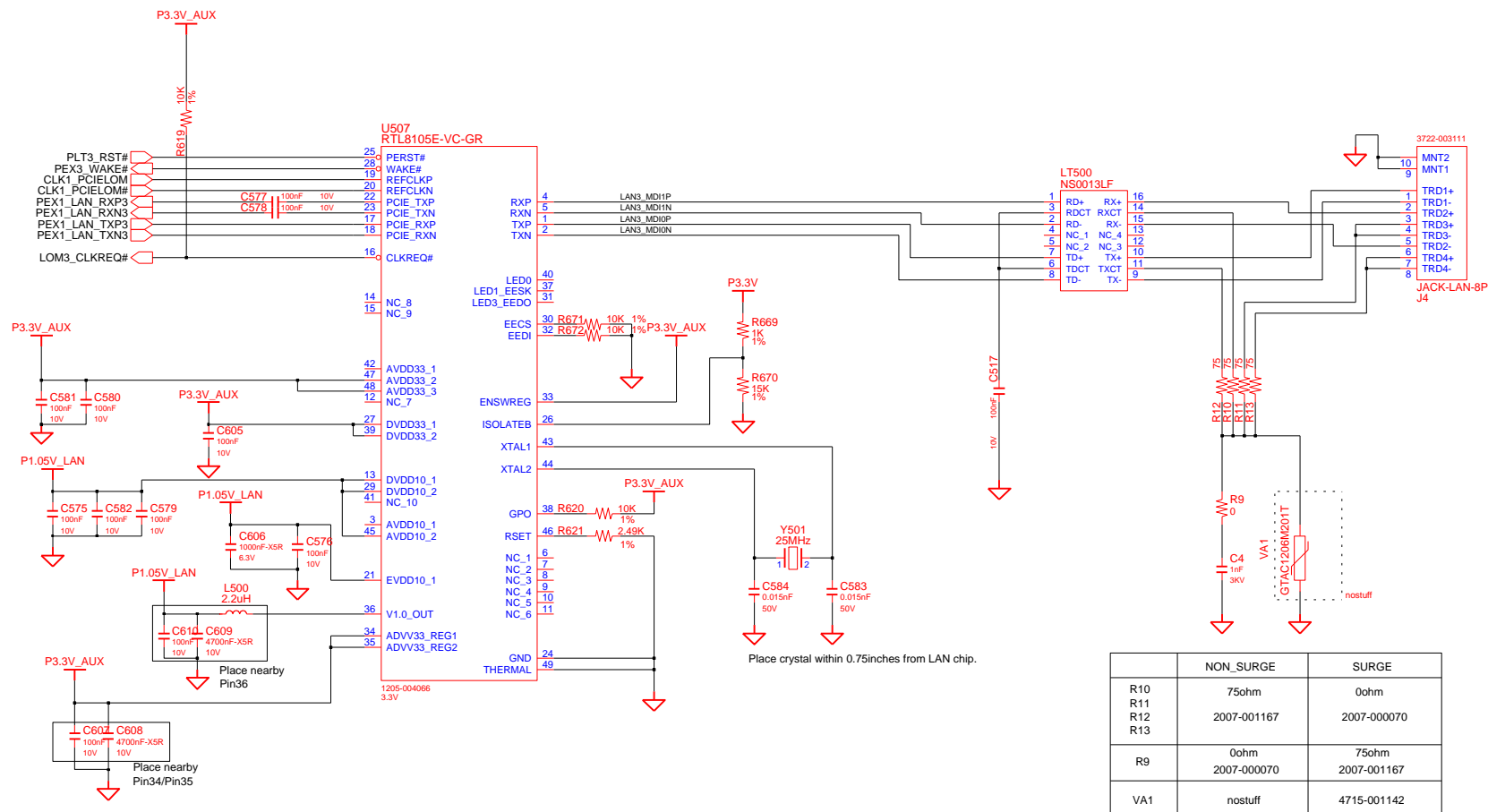
**HEADPHONE****MIC JACK****Internal analog MIC**

INTMIC  
 INTMIC  
 INTMIC  
 INTMIC

DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA AUDIO AUDIO JACK & MIC	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	23 OF 44	

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**Realtek RTL8105E**

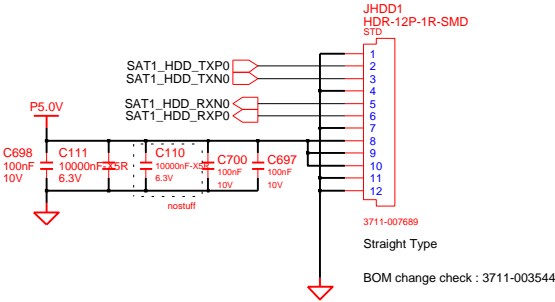
DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR		LAN	
APPROVAL	BL LEE	REV	1.0		RTL8105E	
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	24 OF 44	



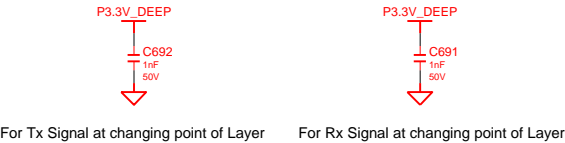
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# SATA I/F CONN

## SATA HDD CONN



For EMI



DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA SATA_DEVICES SATA I/F	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	25 OF 44	

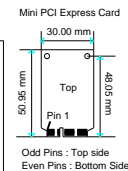
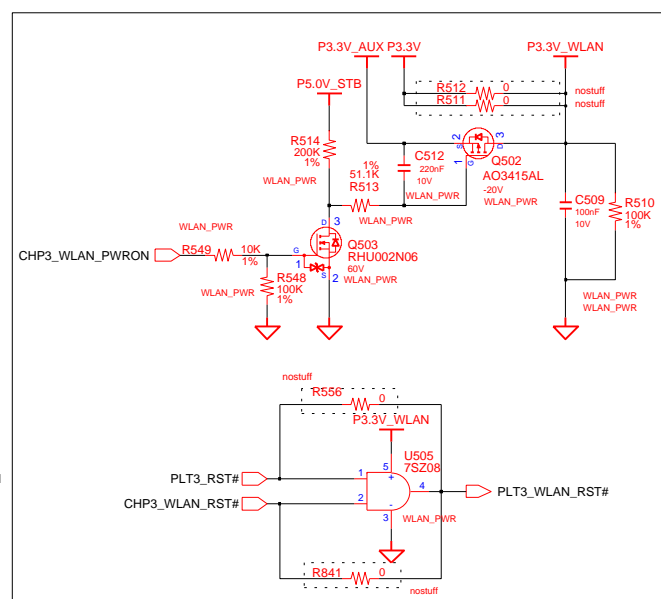
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3709-001470

Near to Mini card Connector

PEM for Half length card

M1 HEAD DIA LENGTH BAG1-01102A

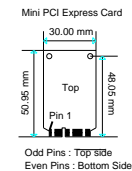


The diagram illustrates the pinout and connections for the J18 EDGE-MINIPCI-E-52P connector. The connector is shown with its 52 pins, and the signals are listed on the right side of the diagram. The signals include:

- WAKE\*
- RSVD\_1
- RSVD\_2
- CLKREQ\*
- GND\_2
- REFCLK\_C3
- REFCLK+
- GND\_3
- SIM\_RSVD\_C8
- SIM\_RSVD\_C4
- GND\_5
- PERNRXP0(mSATA)
- PERP0RXN0(mSATA)
- GND\_7
- GND\_8
- PETN0TXN0(mSATA)
- PETP0TXP0(mSATA)
- GND\_10
- RSVD\_11
- RSVD\_12
- RSVD\_13
- RSVD\_14
- RSVD\_15
- RSVD\_16
- RSVD\_17
- RSVD\_18
- P3.3V
- TV\_SS\_HSPA
- SIM3\_C1VCC
- SIM3\_C2RST
- SIM3\_C3CLK
- SIM3\_C7DATA
- SIM3\_C3CLK
- SIM3\_C2RST
- CHP3\_RFOFF\_HSDPA#
- PLT3\_RST#
- KBC3\_PWRON
- USB3\_MINIPCIE2-
- USB3\_MINIPCIE2+
- M3 HEAD DIA
- M2 HEAD DIA
- TV\_HSP

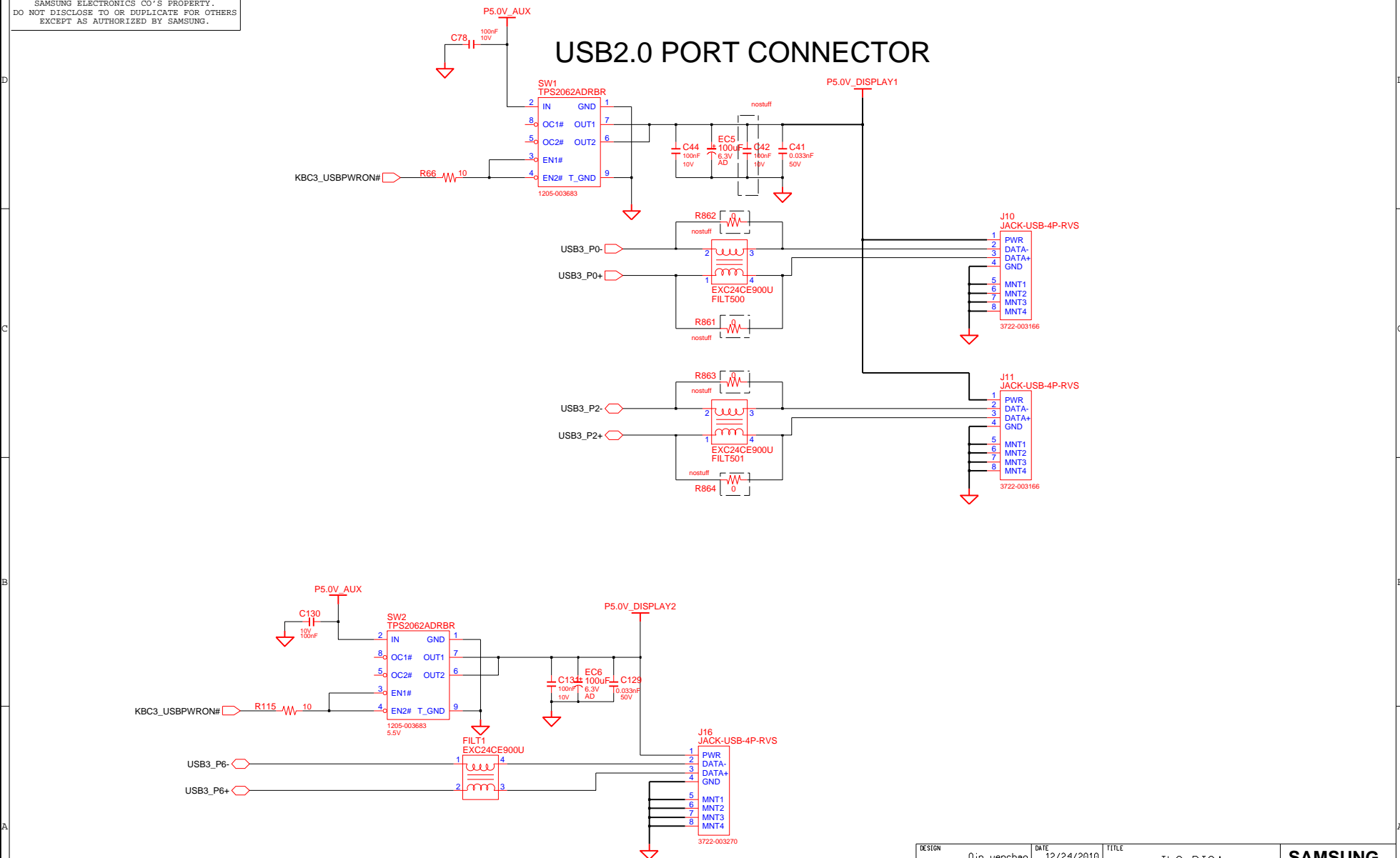
The diagram also shows the connection of the connector to the board, including the P3.3V and TV\_SS\_HSPA signals. The connector is shown with its 52 pins, and the signals are listed on the right side of the diagram. The signals include:

- WAKE\*
- RSVD\_1
- RSVD\_2
- CLKREQ\*
- GND\_2
- REFCLK\_C3
- REFCLK+
- GND\_3
- SIM\_RSVD\_C8
- SIM\_RSVD\_C4
- GND\_5
- PERNRXP0(mSATA)
- PERP0RXN0(mSATA)
- GND\_7
- GND\_8
- PETN0TXN0(mSATA)
- PETP0TXP0(mSATA)
- GND\_10
- RSVD\_11
- RSVD\_12
- RSVD\_13
- RSVD\_14
- RSVD\_15
- RSVD\_16
- RSVD\_17
- RSVD\_18
- P3.3V
- TV\_SS\_HSPA
- SIM3\_C1VCC
- SIM3\_C2RST
- SIM3\_C3CLK
- SIM3\_C7DATA
- SIM3\_C3CLK
- SIM3\_C2RST
- CHP3\_RFOFF\_HSDPA#
- PLT3\_RST#
- KBC3\_PWRON
- USB3\_MINIPCIE2-
- USB3\_MINIPCIE2+
- M3 HEAD DIA
- M2 HEAD DIA
- TV\_HSP

[illegible]

DESIGN	Qin wenchao	DATE	12/24/2010	TITLE ILS_RISA MINI_PCIE.CONN MINI PCI	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR		
APPROVAL	BL LEE	REV	1.0		
MODULE CODE	LAST EDIT		February 23, 2012 11:39:06 AM		
					PART NO. BA41-0XXXXA

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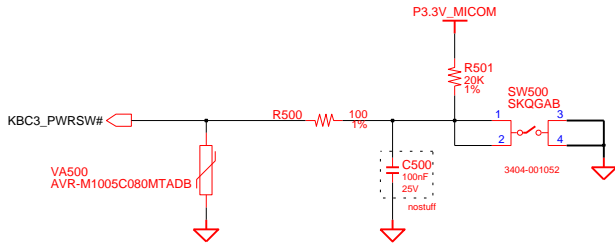


DESIGN		Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA USB_CONN USB PORT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK		Wu shijiang	DEV. STEP	PR			
APPROVAL		BL LEE	REV	1.0			
MODULE CODE			LAST EDIT		February 23, 2012 11:39:06 AM	PAGE	27 OF 44

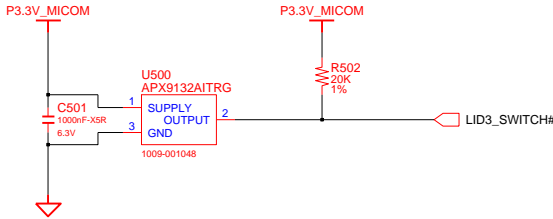
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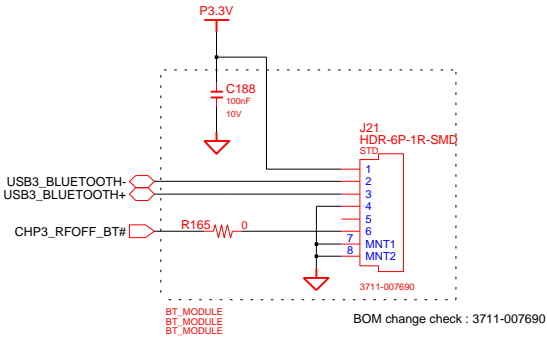
## Power Switch Board Connector



## LID SWITCH

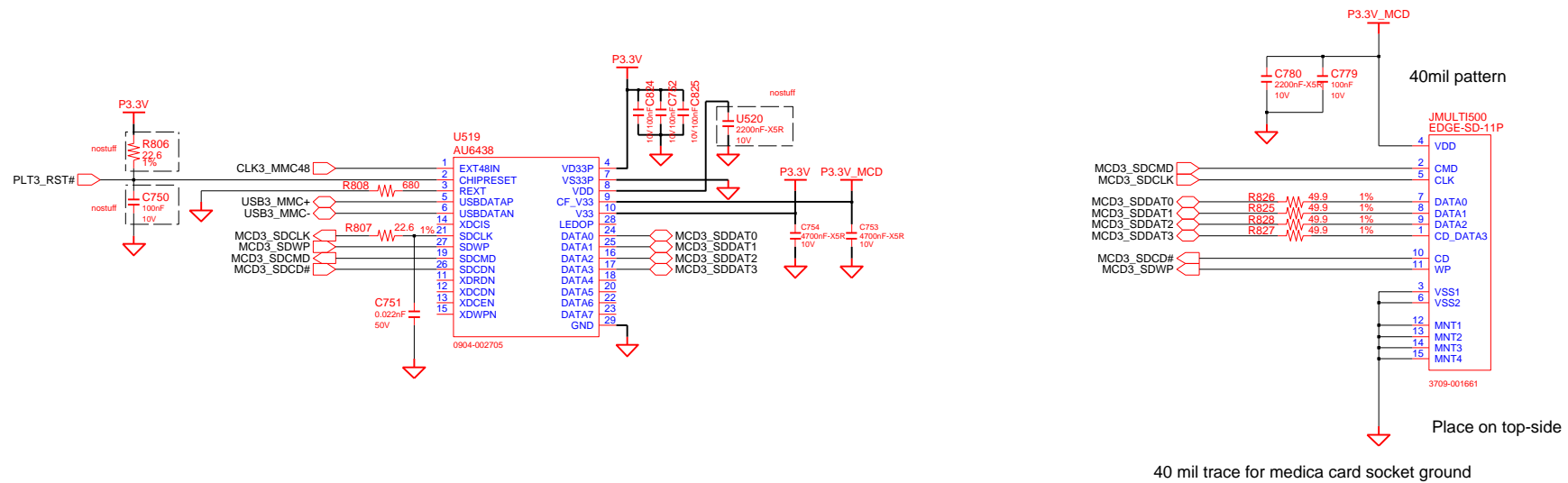


## BLUETOOTH



DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR		USB_DEVICES SB I/F	
APPROVAL	BL LEE	REV	1.0		BLUETOOTH, System B'D I/F	
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	28 OF 44	

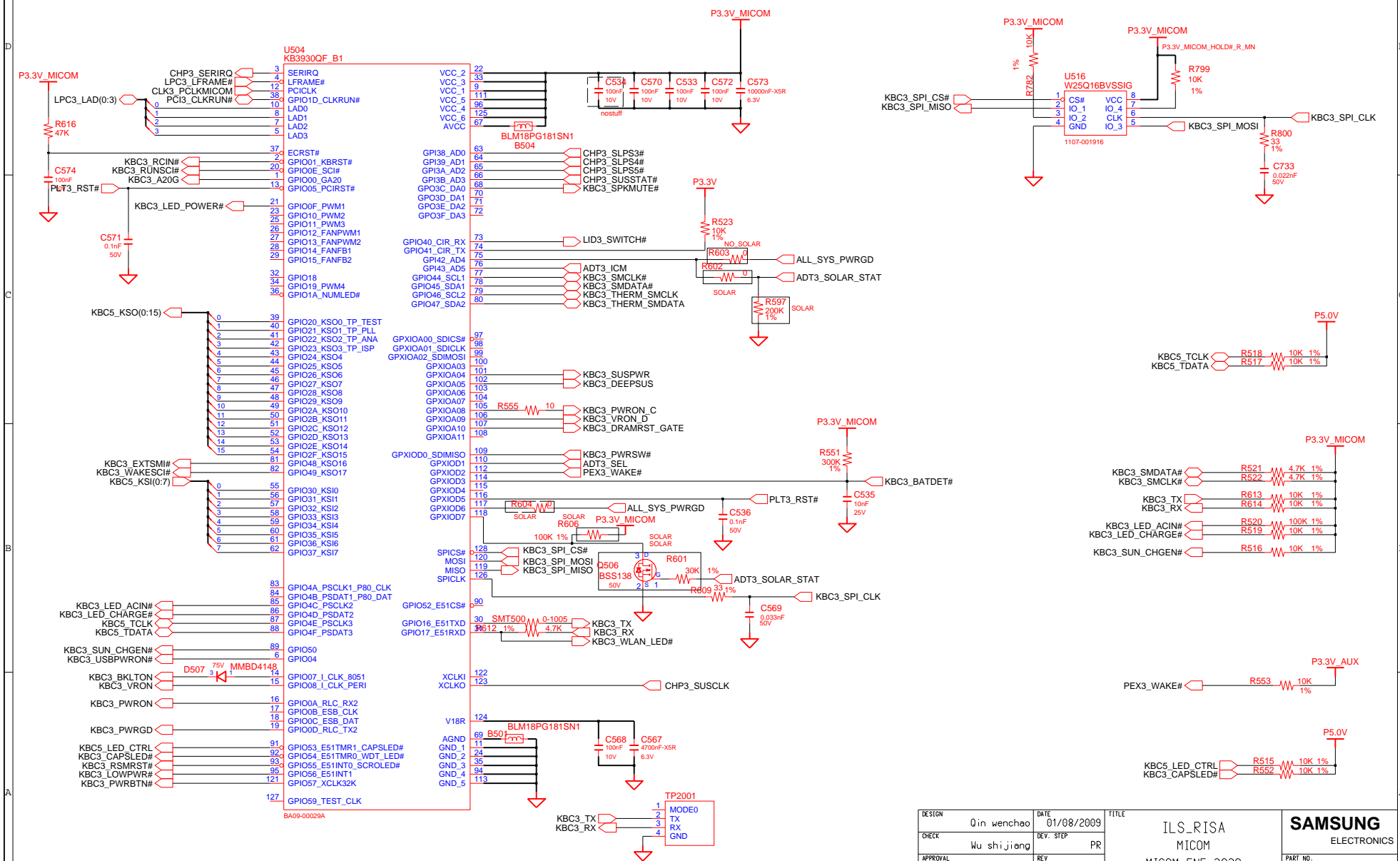
# MMC(AU6438)



DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	REV. STEP	PR		MMC	
APPROVAL	BL LEE	REV	1.0		AUG438	
MODULE CODE		LAST EDIT				
				February 23, 2012 11:39:06 AM	PAGE	29 OF 43

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**MAIN BOARD (MICOM 3930)****BE CAUTION SPI ROM SIZE!!**

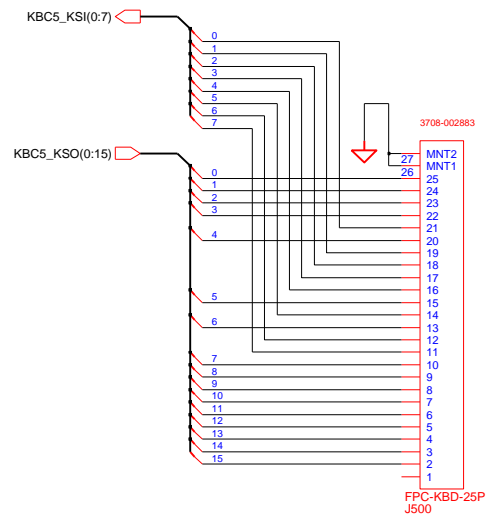
DESIGN	Qin wenchao	DATE	01/08/2009	TITLE	ILS_RISA MICOM MICOM ENE 3930	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	30 OF 44	

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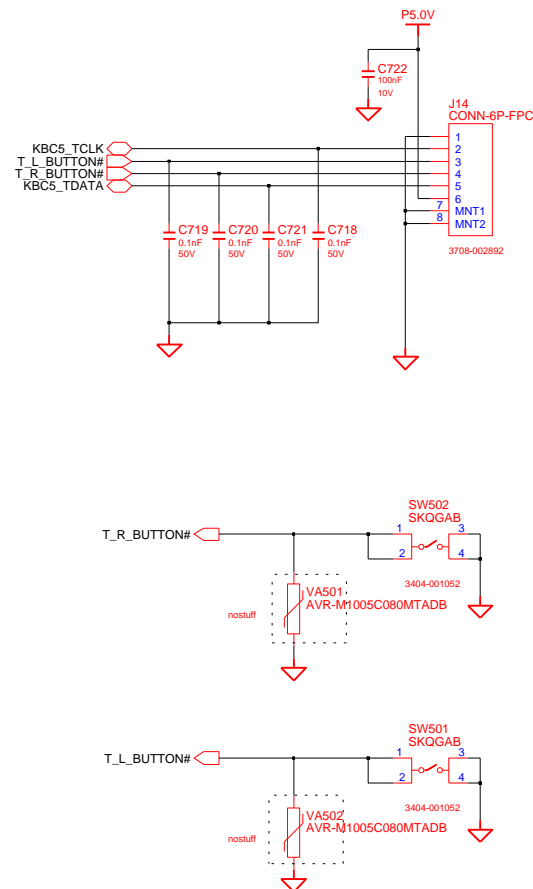
# Micom Glue Logic

## KEYBOARD



Reverse KBD connection as lib. is reversed

## TOUCHPAD

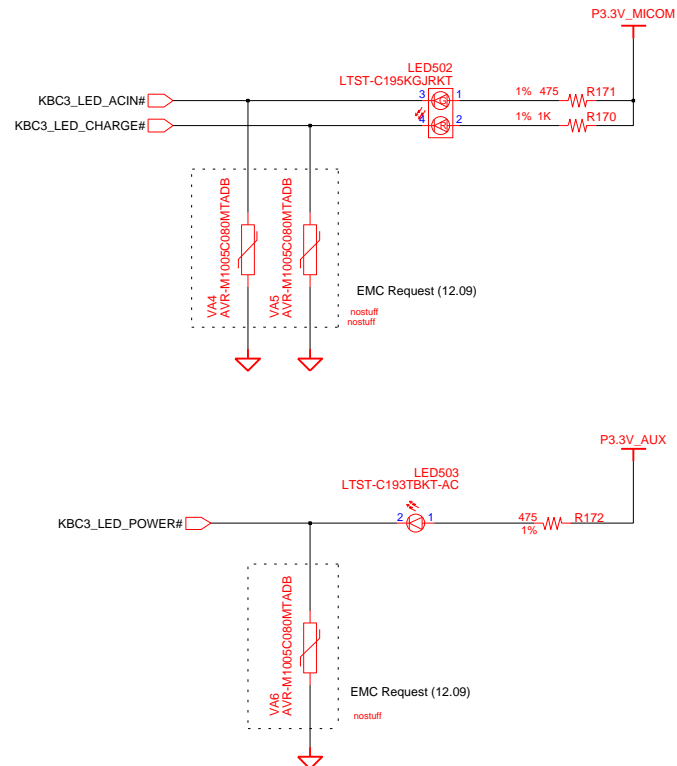
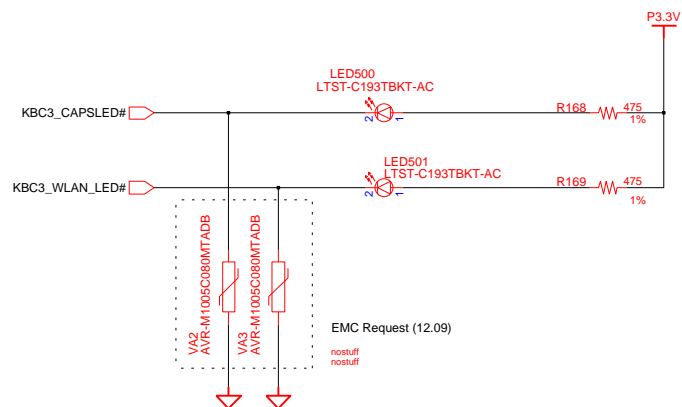


DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA MICOM MICOM GLUE LOGIC	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			PART NO. BA41-0XXXXA
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	31	OF 44

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# LED SWITCH LOGIC

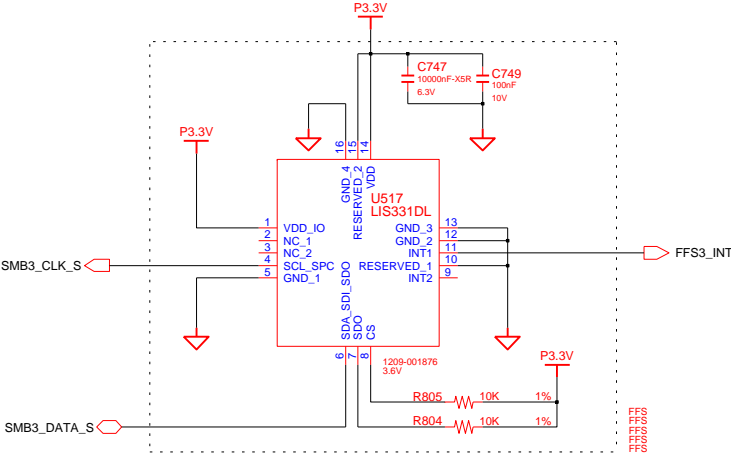


DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			PART NO. BA41-0XXXXA
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	32	OF 44



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**FREE FALL SENSOR**



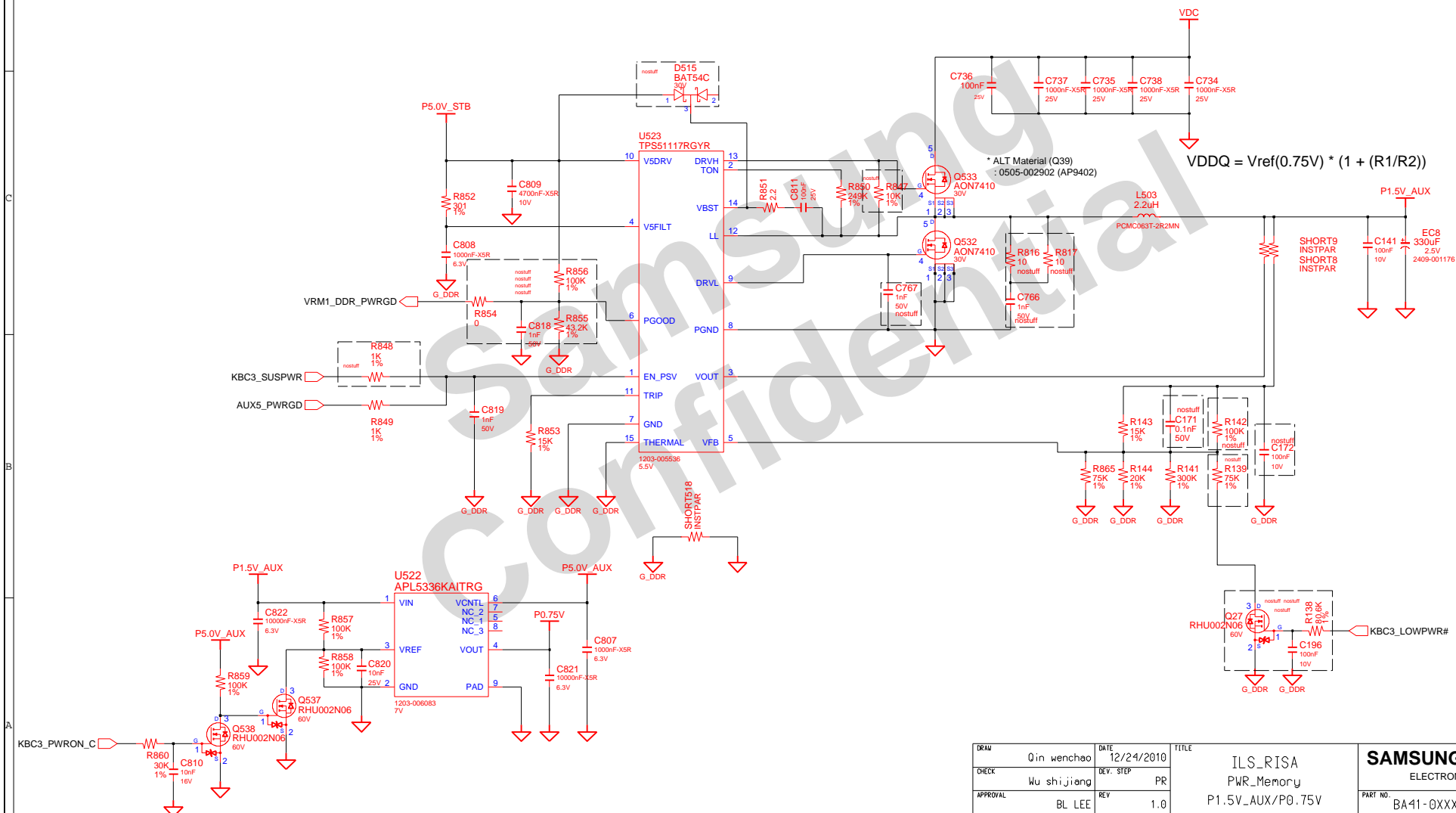
DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA FFS FreeFallSensor	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			PART NO. BA41-0XXXXA
APPROVAL	BL LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	33	OF 44



DRAM	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA Chipset Power P1.05V / P1.8V	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	REV. STEP	PR			
APPROVAL	BL LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	February 23, 2012 11:39:06 AM			
				PAGE	35	OF 44

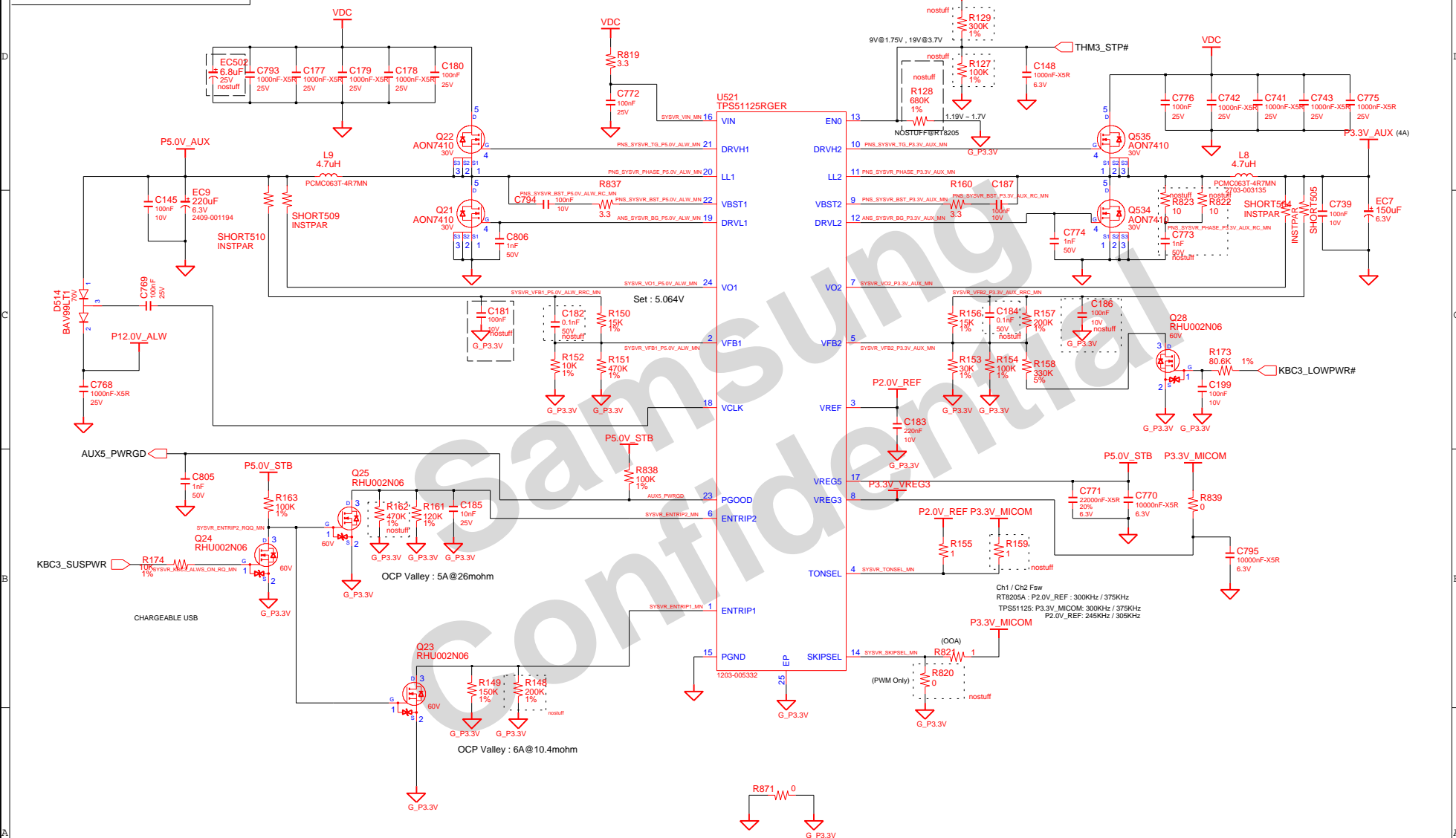
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**DDR3 Power ( P1.5V\_AUX & P0.75V)**

DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR		PWR_Memory	
APPROVAL	BL LEE	REV	1.0		P1.5V_AUX/P0.75V	PART NO.
MODULE CODE	undefined	LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	36	BA41-0XXXXA
					OF	44

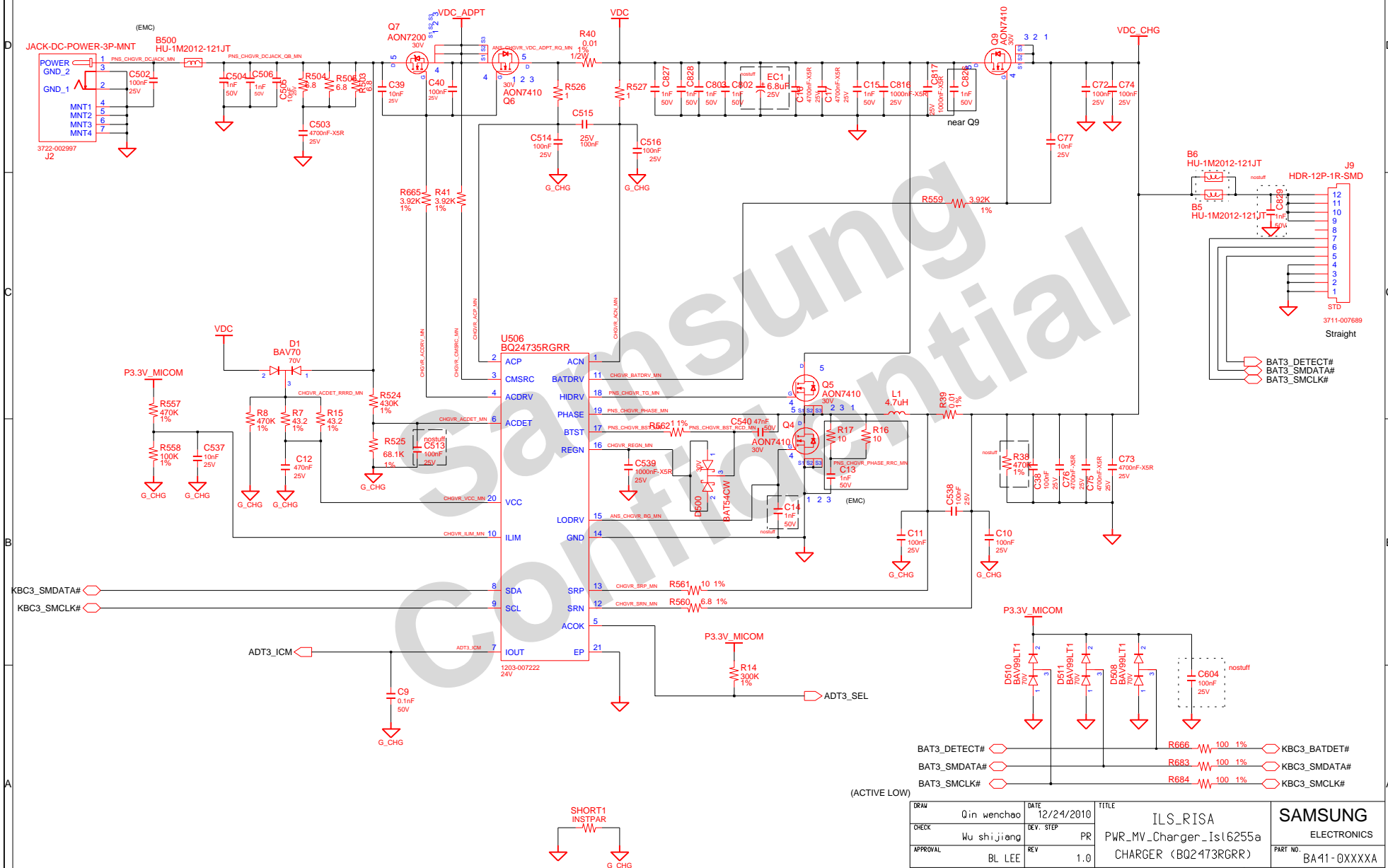
## P3.3V\_AUX & P5.0V\_AUX



DRAM	Qin wenchao	DATE	12/24/2010	TITLE	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	PR			PWR_MV_3V_5V
APPROVAL	BL LEE	REV	1.0			P3.3V_AUX / P5.0V_AUX
MODULE CODE	undefined	LAST EDIT	February 23, 2012 11:39:06 AM			PAGE 37 OF 44
PART NO.					BA41-0XXXXA	

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# CHARGER & POWER MANAGEMENT

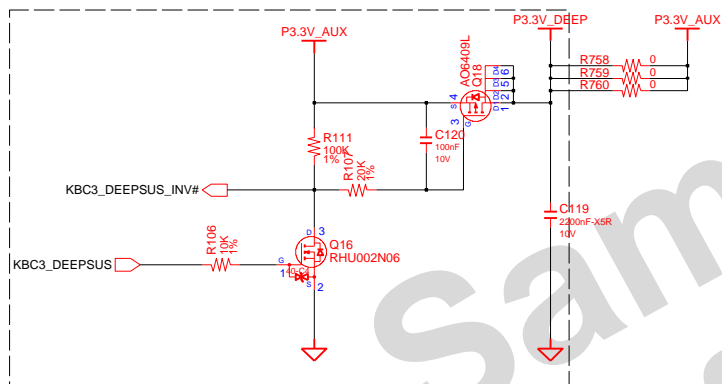
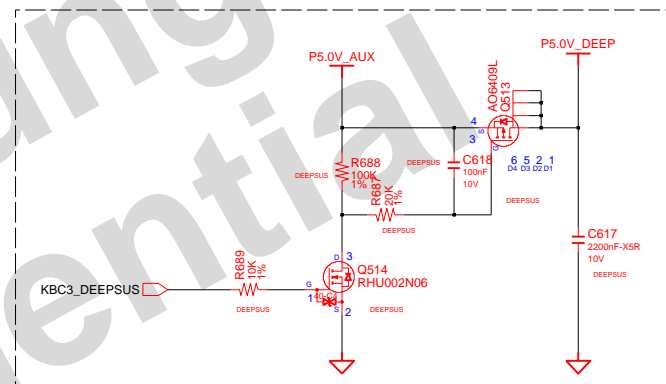


(ACTIVE LOW)

DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	SAMSUNG
CHECK	Wu shijiang	DEV. STEP	PR	PWR_MV_Charger_Ist6255a	CHARGER (BQ2473RGR)	ELECTRONICS
APPROVAL	BL LEE	REV	1.0			PART NO. BA11-0XXXXA
MODULE CODE	undefined	LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	38	OF 44

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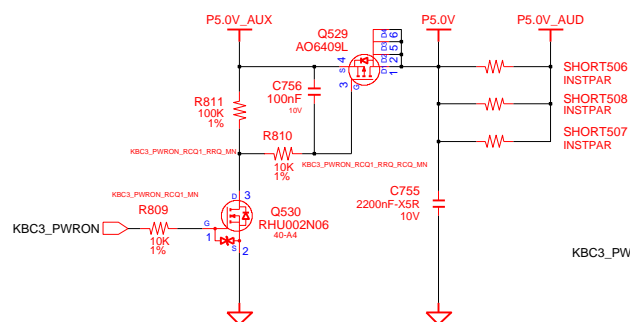
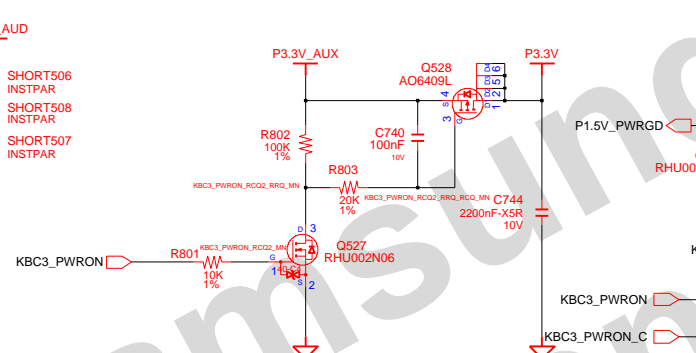
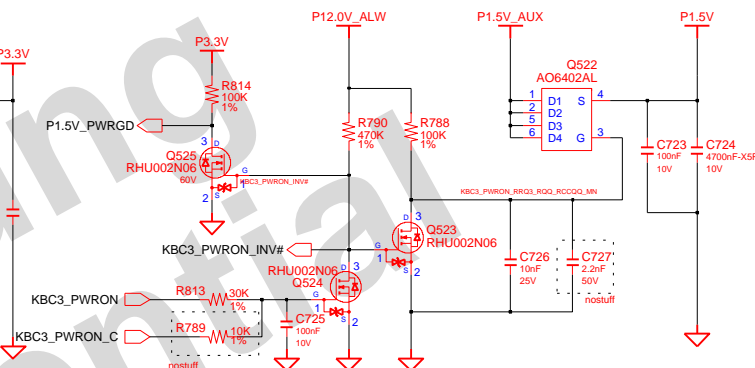
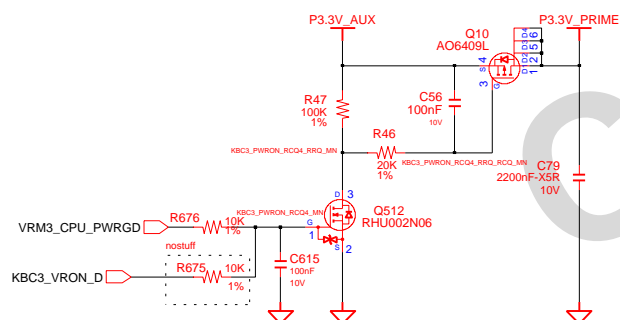
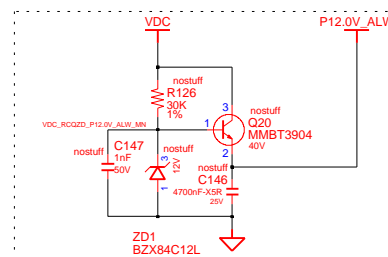
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**Load Switch Control (P3.3V\_DEEP)****Load Switch Control (P5.0V\_DEEP)**

DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA DEEP POWER P3.3V_DEEP/P5.0V_DEEP	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BL LEE	REV	1.0			
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	39 OF 44	

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**Load Switch Control (P5.0V)****Load Switch Control (P3.3V)****Load Switch Control (P1.5V)****Load Switch Control (P3.3V\_PRIME)****P12V\_ALW**

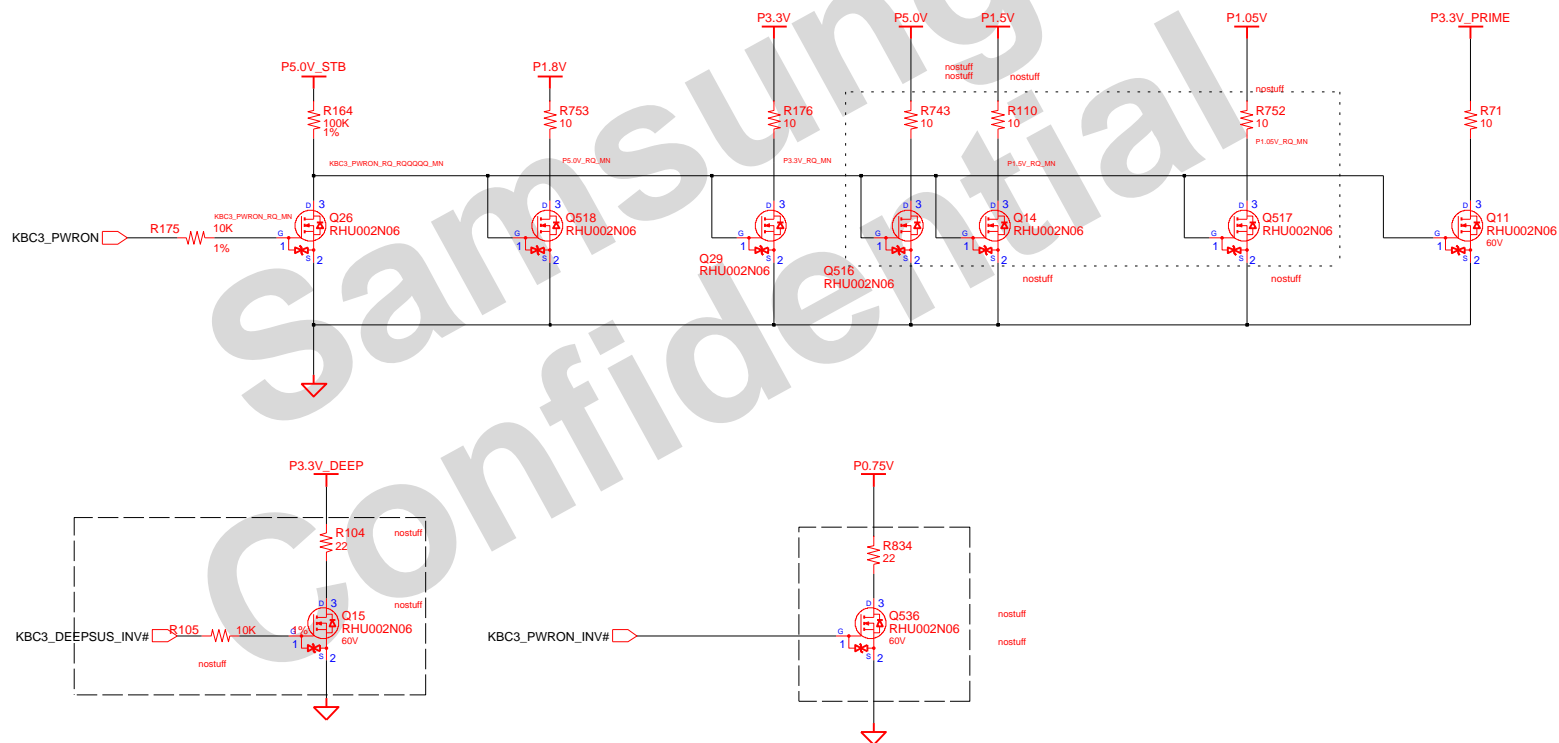
DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR		Switched PWR	
APPROVAL	BL LEE	REV	1.0		Switched PWR	
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	40 OF 44	



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## PWR Discharger



DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA Discharger	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BL LEE	REV	1.0			PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	41	OF 44

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# Solar Cell Logic Board

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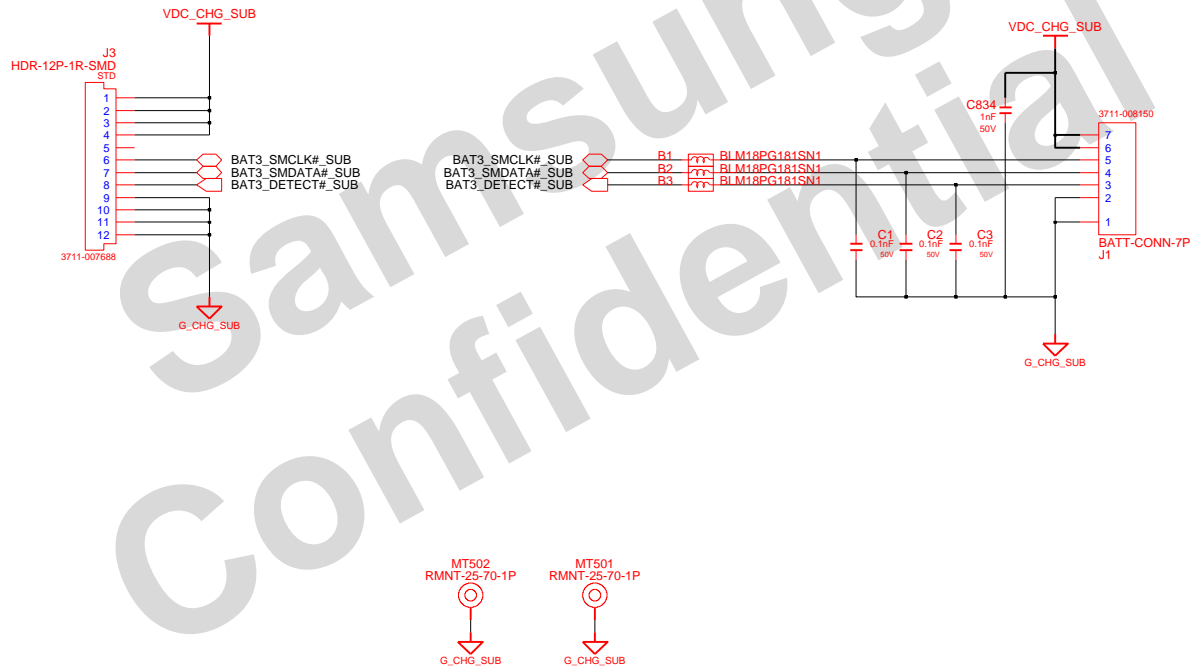
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DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR		Solar Cell	
APPROVAL	BL LEE	REV	1.0		Solar Cell	
MODULE CODE		LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	42	OF 44

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Battery Sub B'd



DRAW	Qin wenchao	DATE	12/24/2010	TITLE	ILS_RISA Battery Sub B'd Battery Sub B'd	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	REV	1.0	PART NO. BA41-0XXXXA
APPROVAL	BL LEE	LAST EDIT	February 23, 2012 11:39:06 AM	PAGE	43	OF 44

